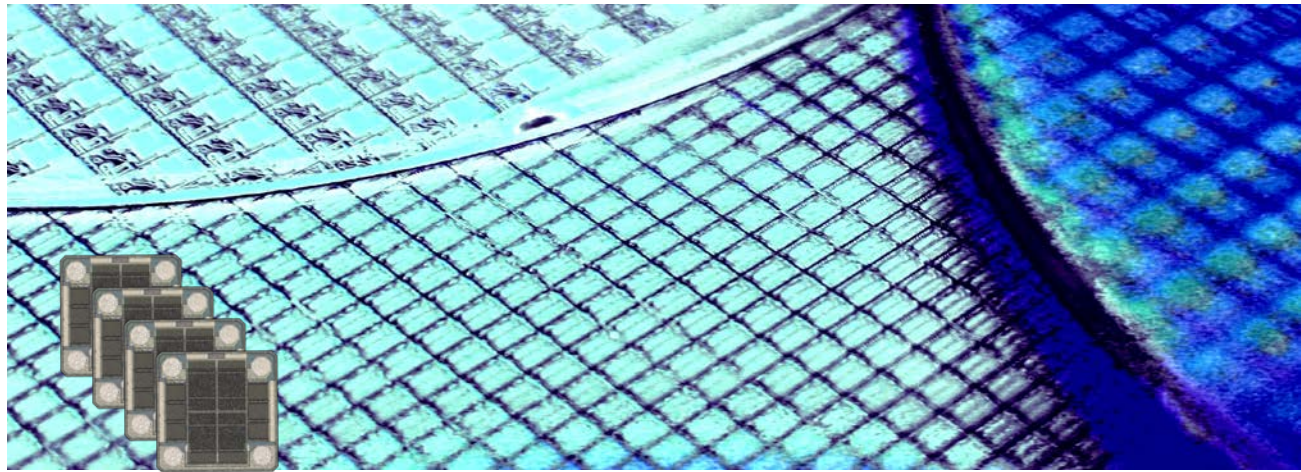


ETSC – Embedded & Wirebond Temperature Silicon Capacitor

Rev 3.2



Key features

- High Operating temperature (200°C)
- Low profile (250µm)
- High stability of capacitance value:
 - ◆ Temperature $\pm 1\%$ (-55°C to +200°C)
 - ◆ Voltage $< 0.1\%$ /Volts
 - ◆ Negligible capacitance loss through ageing
- Low leakage current down to 100pA
- High reliability
- Different Pad finishing available (Al, Au, Ni/Au)

Thanks to the unique IPDiA Silicon capacitor technology, most of the problems encountered in demanding applications can be solved.

Embedded Temperature Silicon Capacitors are dedicated to applications where **reliability** up to **200°C** is the main parameter.

ETSC are the most appropriate solution for Chip On Board, Chip On Foil, Chip On Glass, Chip On Ceramic, flip chip and embedded applications.

This technology features a capacitor integration capability (up to 250nF/mm²) which offers capacitance value similar to X7R dielectric, but with better electrical performances than C0G/NP0 dielectrics, up to **200°C**.

Key applications

- All applications up to 200°C, such as defense, downhole and automotive industries
- High reliability applications
- Replacement of X7R and C0G dielectrics
- Decoupling / Filtering / Charge pump (i.e.: motor management, temperature sensors)
- Downsizing

ETSC provides the highest capacitor **stability** over the full -55°C/+200°C temperature range in the market with a **TC<1%**.

The IPDiA technology offers industry leading performances relative to **Failure rate** with a FIT<0,017.

This technology also offers **high reliability**, up to 10 times better than alternative capacitor technologies, such as Tantalum or MLCC, and eliminates cracking phenomena.

This Silicon based technology is ROHS compliant and compatible with lead free reflow soldering process.

Electrical specification

		Capacitance value					
		10	15	22	33	47	68
Unit	0.1nF	Contact IPDiA Sales	Contact IPDiA Sales	Contact IPDiA Sales	Contact IPDiA Sales	Contact IPDiA Sales	Contact IPDiA Sales
	1nF	10nF/0202 935 124 72C 510	Contact IPDiA Sales	22nF/0203 935 124 72I 522	Contact IPDiA Sales	Contact IPDiA Sales	Contact IPDiA Sales
		100nF/0404 935 124 42F 610	Contact IPDiA Sales	220nF/0505 935 124 42H 622	Contact IPDiA Sales	Contact IPDiA Sales	Contact IPDiA Sales
	0.1µF	1µF/1208 935 124 42S 710	Contact IPDiA Sales	2.2µF/1612 935 124 42V 722	3.3µF/1616 935 124 42Y 733	4.7µF/2016 935 124 42X 747	

(*) Other values on request

(**) For extended temperature range (up to +250°C), see Embedded Xtreme Temperature Silicon Capacitor product (EXSC).

Parameters	Value
Capacitance range	10nF to 4.7µF ^(*)
Capacitance tolerances	±1.5% ^(*)
Operating temperature range	-55 to 200 °C ^(**)
Storage temperatures	- 70 to 215 °C
Temperature coefficient	±1%, from -55 to +200°C
Breakdown Voltage (BV)	90, 50, 30, 20, 11V
Capacitance variation versus RVDC	0.1 % / V (from 0 V to RVDC)
Equivalent Serial Inductor (ESL)	Max 100 pH
Equivalent Serial Resistor (ESR)	Max 0.1Ω
Insulation resistance	50GΩ min @ RVDC, 25°C 20GΩ min @ RVDC, 200°C
Aging	Negligible, < 0.001% / 10000h
Reliability	FIT<0.017 parts / billions hours
Capacitor height	Max 250µm ^(*)

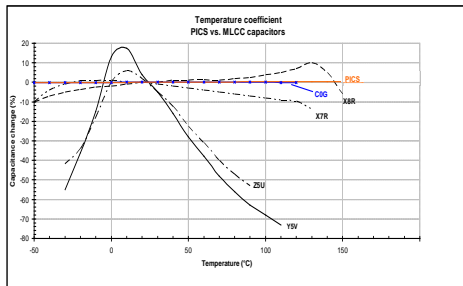


Fig.1 Capacitance change versus temperature variation compared to alternative technologies

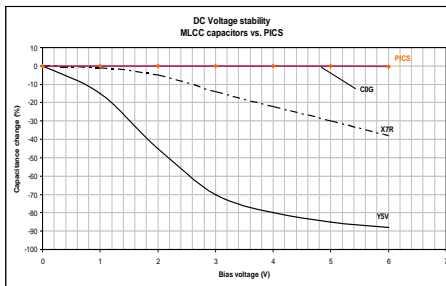


Fig.2 Capacitance change versus voltage variation compared to alternative

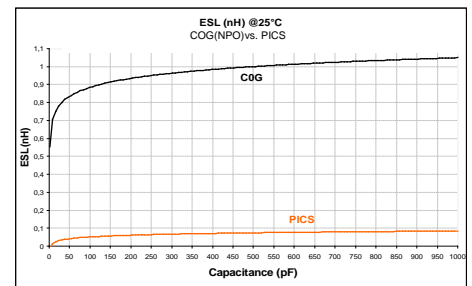


Fig.3 ESL versus capacitance value compared to alternative technologies

Part Number

935.124.

i.e: 100nF/0404 → 935 124 42F 610

B.2. Breakdown Voltage
4 = 11V
1 = 20V
7 = 30V
6 = 50V

S. Size
F = 0404
H = 0505
I = 0302
S = 1208
V = 1216

U Unit
0 = 10f
1 = 0.1p
2 = 1p
3 = 10p
4 = 0.1n

XX → Value
5 = 1n
6 = 10n
7 = 0.1u
8 = 1u
9 = 10u

Value
10
15
22
33
47
68

Termination

Pad finishing in Aluminum (3µm thickness +/-10%), other finishing available such as copper, nickel or gold. Applicable for almost all embedded applications. Parts should be glued with non conductive paste. If conductive glue is used on the backside of the silicon cap, it is strongly recommended to connect the backside and pads 3 & 4 to the same level (GND preferred).

Pinning definition & Outline

pin #	Symbol	Description
1, 2	Signal	Signal
3, 4	GND	Ground

Typ.	0202	0203	0303	0404	0505	1208	1612	1616	2016	
Comp. size	A	0.64 ±0.05	0.64 ±0.05	0.80 ±0.05	1.00 ±0.05	1.25 ±0.05	3.00 ±0.05	4.00 ±0.05	5.00 ±0.05	
	B	0.64 ±0.05	0.80 ±0.05	0.80 ±0.05	1.00 ±0.05	1.25 ±0.05	2.00 ±0.05	3.00 ±0.05	4.00 ±0.05	
	c	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15	
	d				0.72		2.72	3.72	3.72	4.72
	e				0.72		1.72	2.72	3.72	3.72

Packaging

Tape and reel, tray, waffle pack or wafer delivery.

Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.



For more information, please visit: <http://www.ipdia.com>
To contact us, email to: sales@ipdia.com

Date of release: 1st March 2012
Document identifier : CL 431 111 615 144