Surface Mount Multilayer Ceramic Chip Capacitors

KPS Series – Commercial Grade (X7R) Dielectric

The Capacitance Company
KEMET CHARGED.

Overview

KEMET's **KPS** series (**K**EMET **P**ower **S**olutions) utilizes proprietary lead-frame technology to vertically stack and place one or two multilayer ceramic chip capacitors (MLCCs) into a parallel circuit and single compact surface mount package. Stacking allows for up to double the capacitance in the same or smaller design footprint when compared to traditional surface mount MLCC devices. The attached lead-frame mechanically isolates the capacitor/s from the printed circuit board, therefore offering advanced mechanical and thermal stress performance. Isolation also addresses concerns for audible, microphonic noise that may occur when a bias voltage is applied.

Providing up to 10mm of board flex capability, KPS series capacitors are environmentally friendly and in compliance with RoHS legislation. Available in X7R dielectric, these devices are capable of Pb-free reflow profiles and provide lower ESR, ESL and higher ripple current capability when compared to other dielectric solutions.

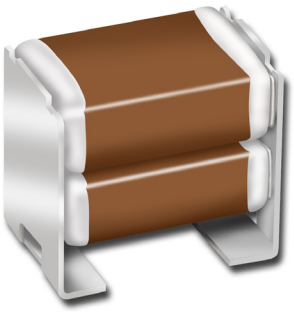
Benefits

- Higher capacitance in the same footprint, greatly reducing board space
- Provides advanced protection against thermal and mechanical stress
- Provides up to 10mm of board flex capability
- Reduces audible, microphonic noise
- Provides extremely low ESR and ESL
- Pb-Free and RoHS compliant
- Capable of Pb-Free reflow profiles
- Non-polar device, minimizing installation concerns
- Tantalum and Electrolytic Alternative
- Automotive Grade (AEC-Q200) under development.

Applications

- Industrial, Automotive, Military, Telecom
- Smoothing circuits
- DC-to-DC convertors
- Power supplies (input/output filters)
- Noise Reduction (piezoelectric/mechanical)
- To increase flex resistance in board flex applications

KPS
KEMET POWER SOLUTIONS



Ordering Information

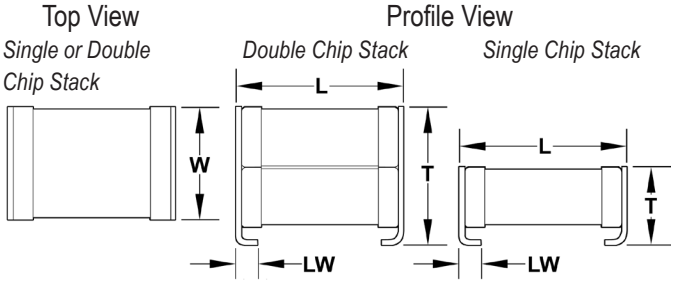
C	2220	C	106	M	5	R	2	C	TU
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance[1]	Voltage	Dielectric	Failure Rate/Design	End Metallization[2]	Packaging/Grade (C-Spec)[3]
	1210 1812 2220	C = Standard	2 Sig. Digits + Number of Zeros	K = ±10% M = ±20%	8 = 10V 4 = 16V 3 = 25V 5 = 50V 1 = 100V A = 250V	R = X7R	1 = KPS Single Chip Stack 2 = KPS Double Chip Stack	C = 100% Matte Sn	TU = 7" Reel Unmarked 7289 = 13" Reel Unmarked

1 Double chip stacks ("2" in the 13th character position of the ordering code) are only available in M (±20%) capacitance tolerance. Single chip stacks ("1" in the 13th character position of the ordering code) are available in K (±10%) or M (±20%) tolerances.

2 Additional termination options may be available. Contact KEMET for details.

3 Additional reeling or packaging options may be available. Contact KEMET for details.

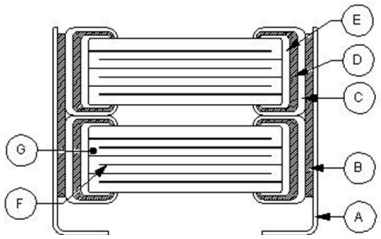
Dimensions – Millimeters (Inches)



Chip Stack	EIA Size Code	Metric Size Code	L Length	W Width	T Thickness	LW Lead Width	Mounting Technique
Single	1210	4532	3.50 (.138) ± 0.30 (.012)	2.60 (.102) ± 0.30 (.012)	3.35 (.132) ± 0.10 (.004)	0.80 (.032) ± 0.15 (.006)	Solder Reflow
	1812	4564	5.00 (.197) ± 0.50 (.020)	3.50 (.138) ± 0.50 (.020)	2.65 (.104) ± 0.35 (.014)	1.10 (.043) ± 0.30 (.012)	
	2220	5650	6.00 (.236) ± 0.50 (.020)	5.00 (.197) ± 0.50 (.020)	3.50 (.138) ± 0.30 (.012)	1.60 (.063) ± 0.30 (.012)	
Double	1210	4532	3.50 (.138) ± 0.30 (.012)	2.60 (.102) ± 0.30 (.012)	6.15 (.242) ± 0.15 (.006)	0.80 (.031) ± 0.15 (.006)	
	1812	4564	5.00 (.197) ± 0.50 (.020)	3.50 (.138) ± 0.50 (.020)	5.00 (.197) ± 0.50 (.020)	1.10 (.043) ± 0.30 (.012)	
	2220	5650	6.00 (.236) ± 0.50 (.020)	5.00 (.197) ± 0.50 (.020)	5.00 (.197) ± 0.50 (.020)	1.60 (.063) ± 0.30 (.012)	

Outline Drawing

Ref	Name	Material
A	Leadframe	Phosphor Bronze - Alloy 510
B	Leadframe Attach	High Temp Solder
C	Termination	Cu
D		Ni
E		Sn
F	Electrode	Ni
G	Dielectric	$BaTiO_3$



Qualification/Certification

Commercial grade products meet or exceed the performance and reliability standards outlined in Table 4 - Performance and Reliability of this specification.

Environmental Compliance

RoHS PRC (Peoples Republic of China) compliant

Electrical Parameters/Characteristics

Operating Temperature Range:	-55°C to +125°C
Capacitance Change with Reference to +25°C and 0 Vdc Applied (TCC):	±15%
Aging Rate (Max % Cap Loss/Decade Hour):	3.5%
Dielectric Withstanding Voltage:	250% of rated voltage (5 ± 1 seconds and charge/discharge not exceeding 50mA)
Dissipation Factor (DF) Maximum Limits @ 25ºC:	5% (10V), 3.5% (16V & 25V) and 2.5% (50V to 200V)
Insulation Resistance (IR) Limit @ 25°C:	See Insulation Resistance Limit Table page 3

To obtain IR limit, divide MΩ-µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.
Capacitance and Dissipation Factor (DF) measured under the following conditions:

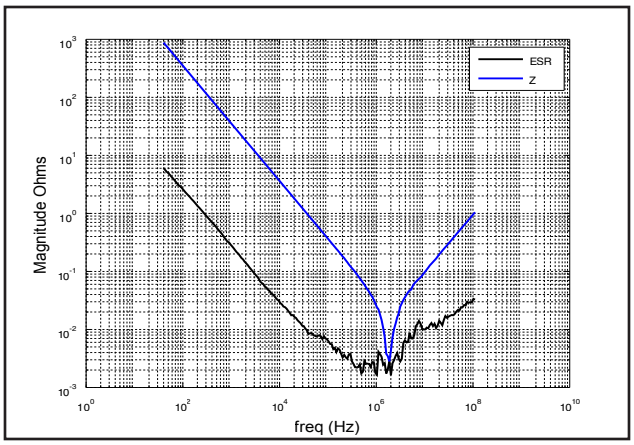
1kHz ± 50Hz and 1.0 ± 0.2 Vrms if capacitance ≤10µF
120Hz ± 10Hz and 0.5 ± 0.1 Vrms if capacitance >10µF

Insulation Resistance Limit Table (X7R Dielectric)

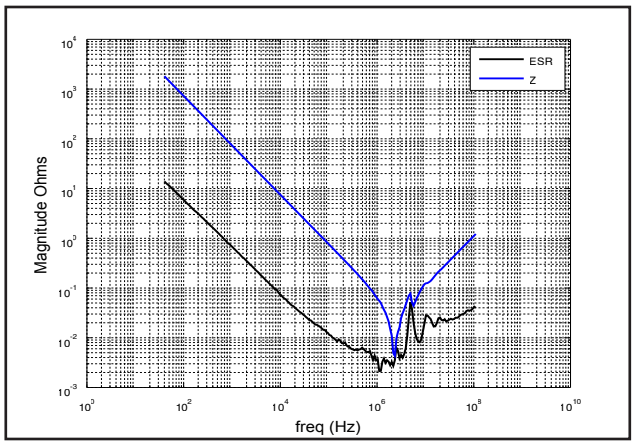
EIA Case Size	1000 megohm microfarads or 100GΩ	500 megohm microfarads or 10GΩ
1210	< 0.39µF	≥ 0.39µF
1812	< 2.2µF	≥ 2.2µF
2220	< 10µF	≥ 10µF

Impedance and ESR

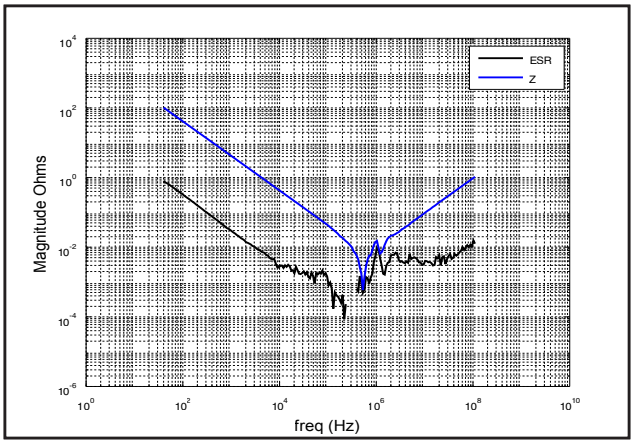
Z and ESR C1210C475M5R1C



Z and ESR C2220C225MAR2C

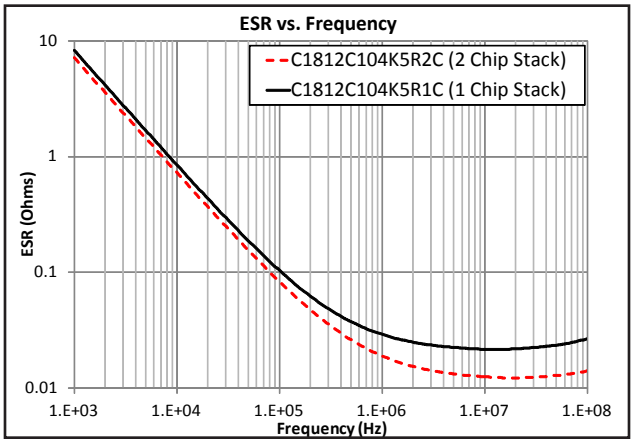


Z and ESR C2220C476M3R2C

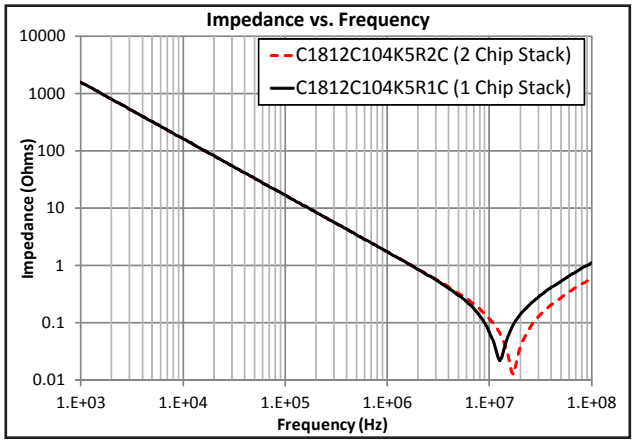


Electrical Characteristics

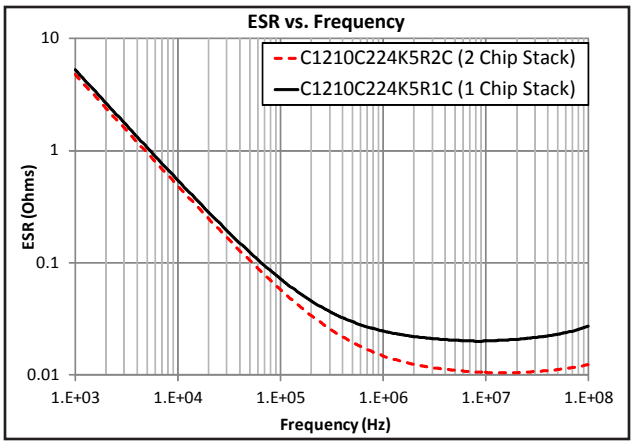
ESR - 1812, .1µF, 50V X7R



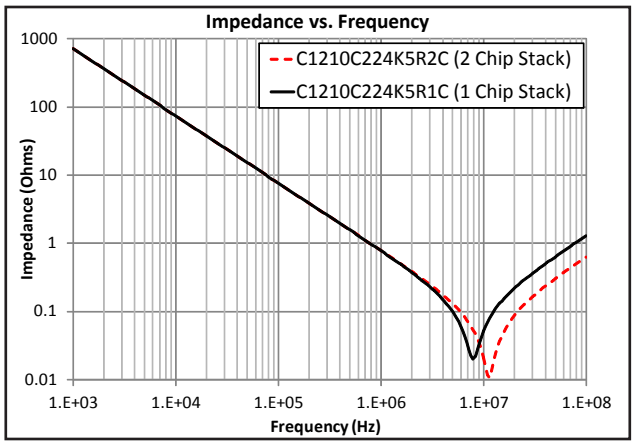
Impedance - 1812, .1µF, 50V X7R



ESR - 1210, .22µF, 50V X7R

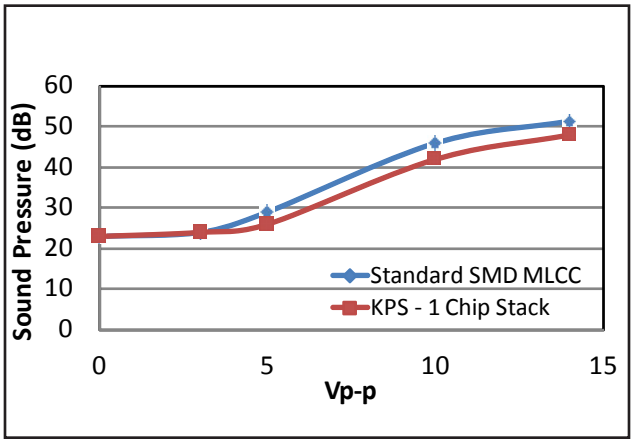


Impedance - 1210, .22µF, 50V X7R

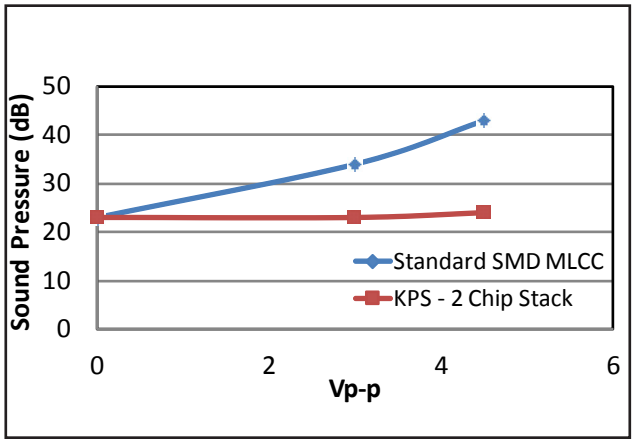


Electrical Characteristics con't

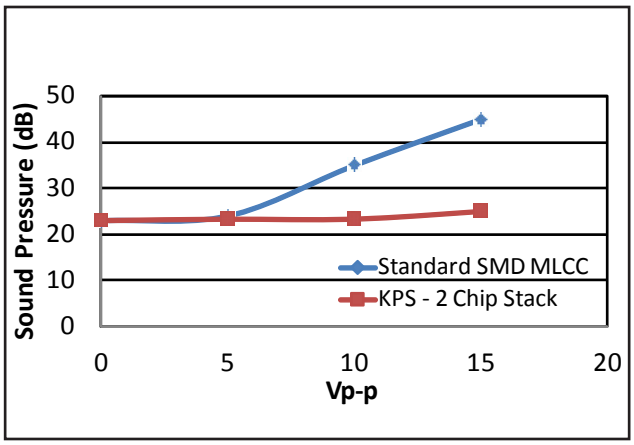
Microphonics - 1210, 4.7µF, 50V, X7R



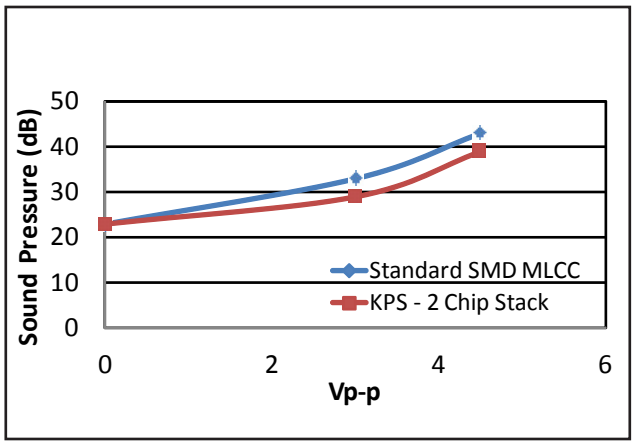
Microphonics - 2220, 22µF, 50V, X7R



Microphonics - 2220, 47µF, 25V, X7R

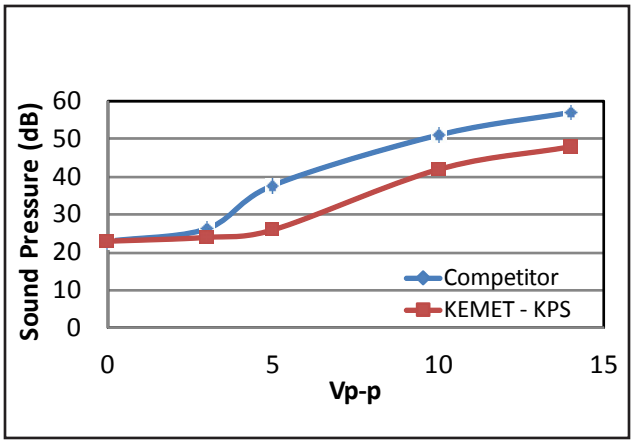


Microphonics - 1210, 22µF, 25V, X7R

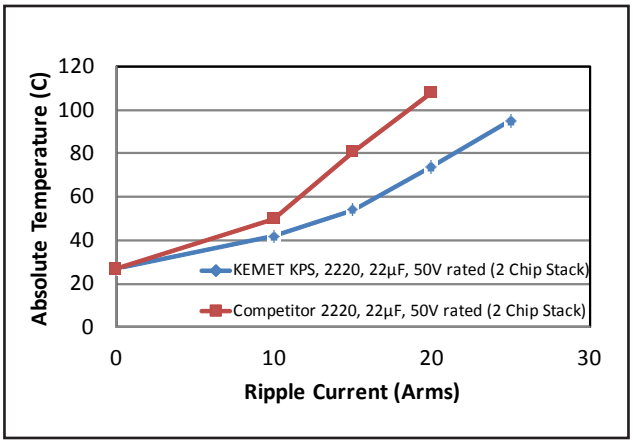


Competitive Comparision

Microphonics - 1210, 4.7µF, 50V, X7R



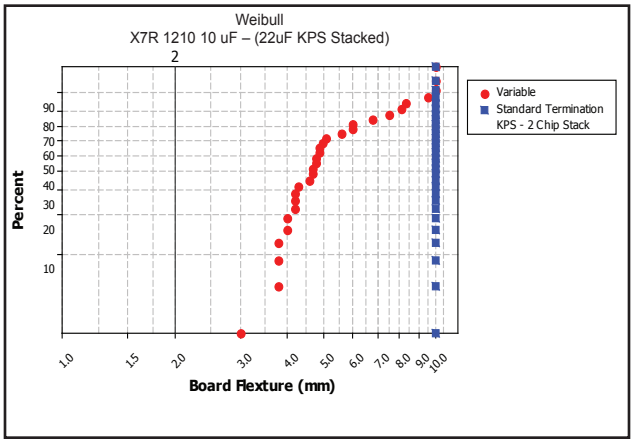
Ripple Current (Arms) 2220, 22µF, 50V



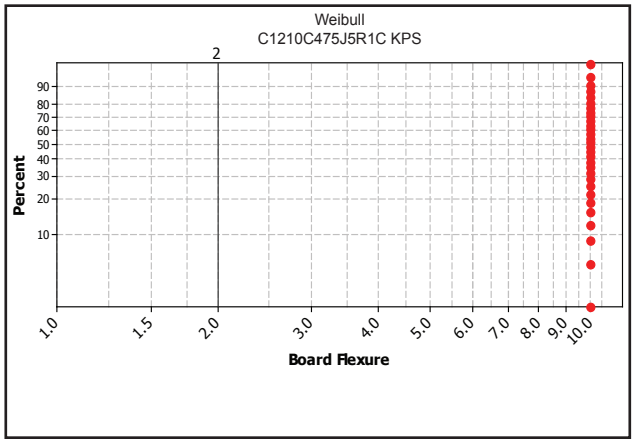
Note: Refer to Table 4 for test method.

Electrical Characteristics con't

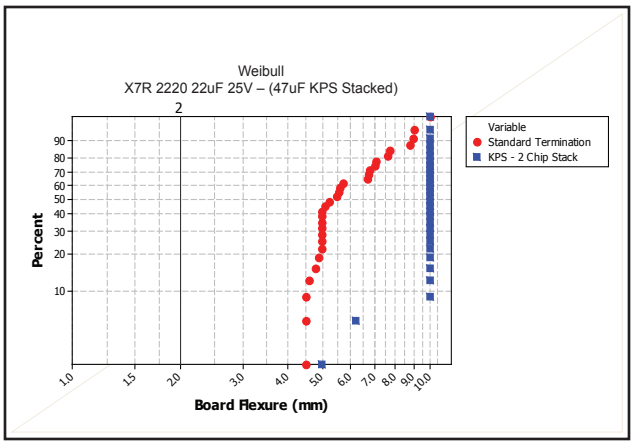
Board Flex vs. Termination Type



Board Flexure to 10mm



Board Flex vs. Termination Type



Board Flexure to 10mm

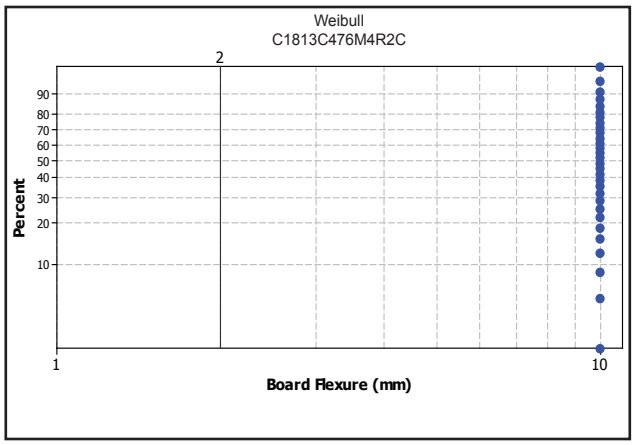


Table 1 – (1210 - 2220 Case Sizes) Dielectric

Cap pF	Cap Code	Series		C1210						C1812					C2220				
		Voltage Code		8	4	3	5	1	A	4	3	5	1	A	4	3	5	1	A
		Voltage		10	16	25	50	100	250	16	25	50	100	250	16	25	50	100	250
		Cap Tolerance		Product Availability and Chip Thickness Codes - See Table 2 for Chip Thickness Dimensions															
Single Chip Stack																			
0.10 uF	104	K	M	FV	FV	FV	FV	FV	FV	GP	GP	GP	GP	GP	JS	JS	JS	JS	JS
0.22 uF	224	K	M	FV	FV	FV	FV	FV		GP	GP	GP	GP	GP	JS	JS	JS	JS	JS
0.47 uF	474	K	M	FV	FV	FV	FV	FV		GP	GP	GP	GP	GP	JS	JS	JS	JS	JS
1.0 uF	105	K	M	FV	FV	FV	FV	FV		GP	GP	GP	GP		JS	JS	JS	JS	JS
2.2 uF	225	K	M	FV	FV	FV	FV	FV		GP	GP	GP			JS	JS	JS	JS	
3.3 uF	335	K	M	FV	FV	FV	FV			GP	GP	GP			JS	JS	JS	JS	
4.7 uF	475	K	M	FV	FV	FV	FV			GP	GP	GP			JS	JS	JS		
10 uF	106	K	M	FV	FV	FV				GP	GP				JS	JS	JS		
15 uF	156	K	M	FV											JS	JS			
22 uF	226	K	M	FV											JS	JS			
33 uF	336	K	M																
47 uF	476	K	M																
100 uF	107	K	M																
Double Chip Stack																			
0.10 uF	104		M	FW	FW	FW	FW	FW	FW	GR	GR	GR	GR	GR	JR	JR	JR	JR	JR
0.22 uF	224		M	FW	FW	FW	FW	FW	FW	GR	GR	GR	GR	GR	JR	JR	JR	JR	JR
0.47 uF	474		M	FW	FW	FW	FW	FW		GR	GR	GR	GR	GR	JR	JR	JR	JR	JR
1.0 uF	105		M	FW	FW	FW	FW	FW		GR	GR	GR	GR	GR	JR	JR	JR	JR	JR
2.2 uF	225		M	FW	FW	FW	FW	FW		GR	GR	GR	GR		JR	JR	JR	JR	JR
3.3 uF	335		M	FW	FW	FW	FW			GR	GR	GR	GR		JR	JR	JR	JR	
4.7 uF	475		M	FW	FW	FW	FW	FW		GR	GR	GR			JR	JR	JR	JR	
10 uF	106		M	FW	FW	FW	FW			GR	GR	GR			JR	JR	JR		
22 uF	226		M	FW	FW	FW				GR	GR				JR	JR	JR		
33 uF	336		M	FW											JR	JR			
47 uF	476		M	FW											JR	JR			
100 uF	107		M																
220 uF	227		M																
Cap pF	Cap Code	Voltage		10	16	25	50	100	250	16	25	50	100	250	16	25	50	100	250
		Voltage Code		8	4	3	5	1	A	4	3	5	1	A	4	3	5	1	A
		Series		C1210						C1812					C2220				

Table 2 – Chip Thickness / Packaging Quantities

Thickness Code	Chip Size	Thickness ± Range (mm)	Qty per Reel 7" Plastic	Qty per Reel 13" Plastic
FV	1210	3.35 ± 0.10	600	2000
FW	1210	6.15 ± 0.15	300	1000
GP	1812	2.65 ± 0.35	500	2000

C	2220	C	106	M	5	R	2	C	TU
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance[1]	Voltage	Dielectric	Failure Rate/Design	End Metallization[2]	Packaging/Grade (C-Spec)[3]
	1210 1812 2220	C = Standard	2 Sig. Digits + Number of Zeros	K = ±10% M = ±20%	8 = 10V 4 = 16V 3 = 25V 5 = 50V 1 = 100V A = 250V	R = X7R	1 = KPS Single Chip Stack 2 = KPS Double Chip Stack	C = 100% Matte Sn	TU = 7" Reel Unmarked 7289 = 13" Reel Unmarked

Soldering Process

- *Recommended Soldering Technique*

  Mounting technique is limited to solder reflow only.
- *Recommended Soldering Profile*

  KEMET recommends following the guidelines outlined in IPC/JEDEC J-STD-020D.1

Table 3 – Chip Capacitor Land Pattern Design Recommendations per IPC-7351

EIA Size Code	Metric Size Code	Median (Nominal) Land Protrusion (mm)		
		X	Y	C
1210	3225	1.75	1.14	3.00
1812	4532	2.87	1.35	4.39
2220	5650	4.78	2.08	5.38

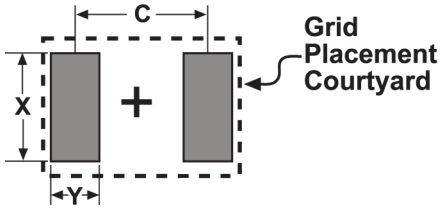
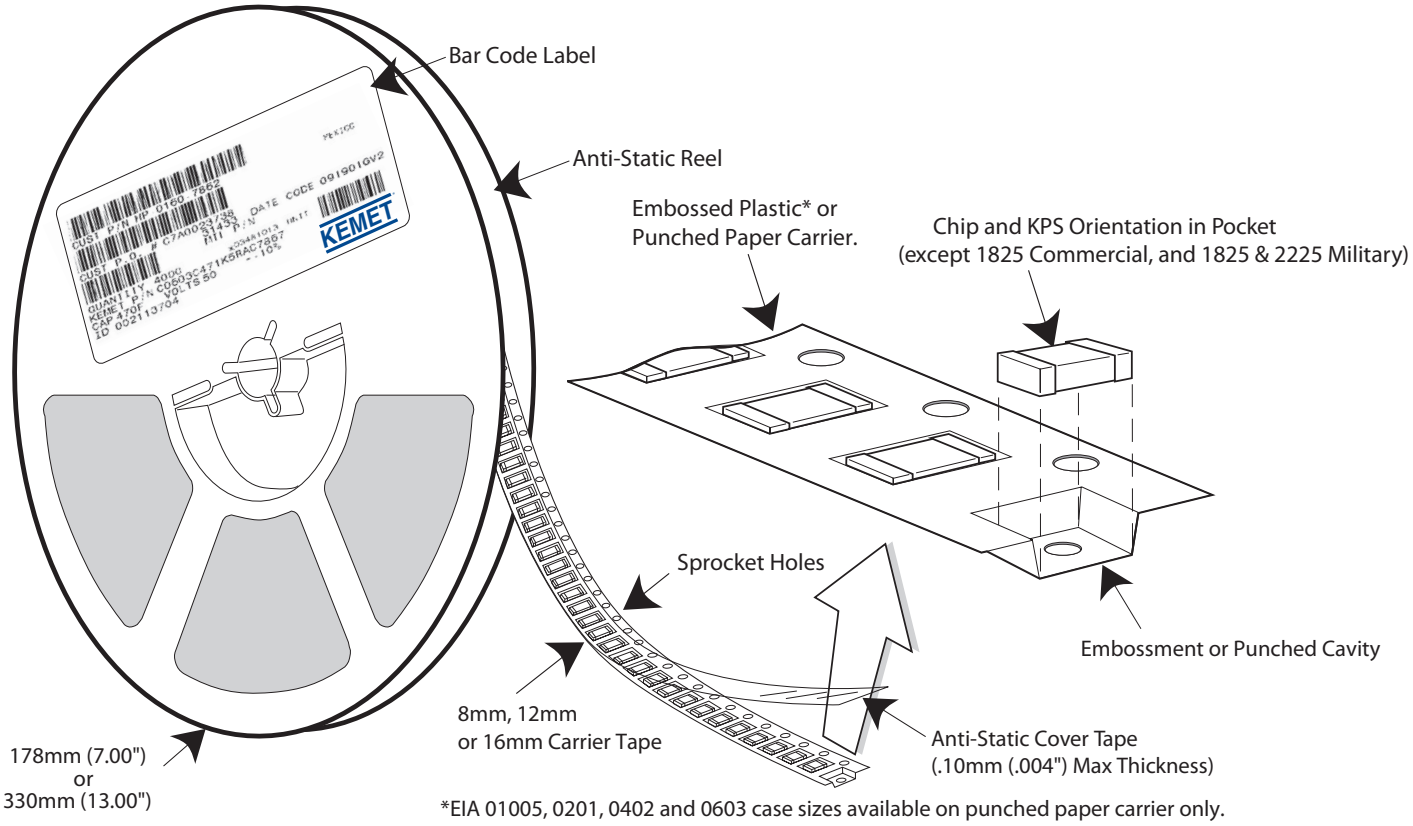


Table 4 – Performance & Reliability: Test Methods and Conditions

Stress	Reference	Test or Inspection Method
Ripple Current	Heat Generation ΔT : 20°C max.	Reflow solder the capacitor onto a PC board and apply voltage with 10kHz~1Mhz sine curve. (Ripple voltage must be < rated voltage)
Terminal Strength	JIS-C-6429	Appendix 1, Note:Force of 1.8kg for 60 seconds.
Board Flex	JIS-C-6429	Appendix 2, Note:2mm (min) for all except 3mm for C0G.
Solderability	J-STD-002	Magnification 50X. Conditions:
		a) Method B, 4 hrs @ 155°C, dry heat @ 235°C
		b) Method B @ 215°C category 3
		c) Method D, category 3 @ 260°C
Temperature Cycling	JESD22 Method JA-104	1000 Cycles (-55°C to +125°C), Measurement at 24 hrs. +/- 2 hrs after test conclusion.
Biased Humidity	MIL-STD-202 Method 103	Load Humidity: 1000 hours 85°C/85%RH and Rated Voltage.Add 100K ohm resistor. Measurement at 24 hrs. +/- 2 hrs after test conclusion.
		Low Volt Humidity:1000 hours 85C°/85%RH and 1.5V.Add 100K ohm resistor. Measurement at 24 hrs. +/- 2 hrs after test conclusion.
Moisture Resistance	MIL-STD-202 Method 106	t = 24 hours/cycle.Steps 7a & 7b not required.Unpowered. Measurement at 24 hrs. +/- 2 hrs after test conclusion.
Thermal Shock	MIL-STD-202 Method 107	-55°C/+125°C.Note: Number of cycles required-300, Maximum transfer time-20 seconds, Dwell time-15 minutes.Air-Air.
High Temperature Life	MIL-STD-202 Method 108	1000 hours at 125°C (85°C for X5R, Z5U and Y5V) with 1.5X rated voltage applied.
Storage Life	MIL-STD-202 Method 108	150°C, 0VDC, for 1000 Hours.
Mechanical Shock	MIL-STD-202 Method 213	Figure 1 of Method 213, Condition F.
Resistance to Solvents	MIL-STD-202 Method 215	Add Aqueous wash chemical - OKEM Clean or equivalent.

Tape & Reel Packaging Information

KEMET offers Multilayer Ceramic Chip Capacitors packaged in 8mm, 12mm and 16mm tape on 7" and 13" reels in accordance with EIA standard 481. This packaging system is compatible with all tape fed automatic pick and place systems. See Table 2 for details on reeling quantities for commercial chips.



*EIA 01005, 0201, 0402 and 0603 case sizes available on punched paper carrier only.

Table 5 - Carrier Tape Configuration (mm)

EIA Case Size	Tape size (W)*	Pitch (P_1)*
01005 - 0402	8	2
0603 - 1210	8	4
1805 - 1808	12	4
≥ 1812	12	8
KPS 1210	12	8
KPS 1812 & 2220	16	12
Array 0508 & 0612	8	4

**Refer to Figure 1 for W and P_1 carrier tape reference locations.*

**Refer to Table 4 for tolerance specifications.*

Figure 1: Embossed (Plastic) Carrier Tape Dimensions

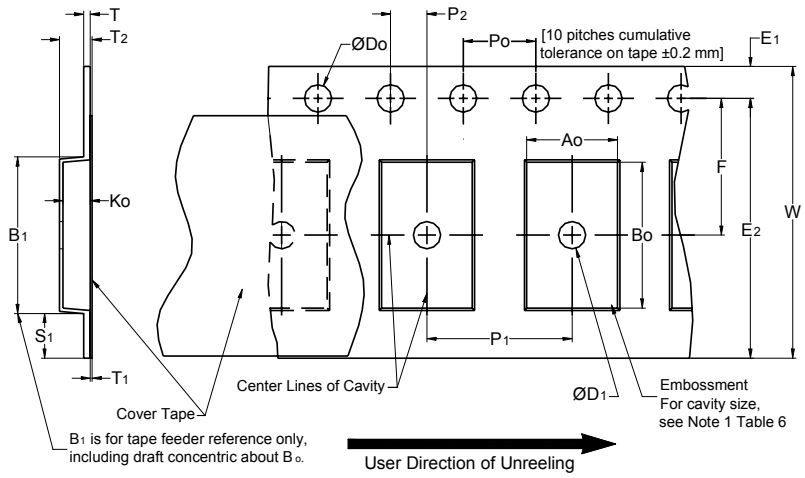


Table 6 - Embossed (Plastic) Carrier Tape Dimensions

(Metric will govern)

Constant Dimensions — Millimeters (Inches)									
Tape Size	D_0	D_1 Min. Note 1	E_1	P_0	P_2	R Ref. Note 2	S_1 Min. Note 3	T Max.	T_1 Max.
8mm	1.5 +0.10/-0.0 (0.059 +0.004/-0.0)	1.0 (0.039)	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	2.0 ± 0.05 (0.079 ± 0.002)	25.0 (0.984)	0.600 (0.024)	0.600 (0.024)	0.100 (0.004)
12mm		1.5 (0.059)				30 (1.181)			
16mm									

Variable Dimensions — Millimeters (Inches)								
Tape Size	Pitch	B_1 Max. Note 4	E_2 Min.	F	P_1	T_2 Max	W Max	A_0,B_0 & K_0
8mm	Single (4mm)	4.35 (0.171)	6.25 (0.246)	3.5 ± 0.05 (0.138 ± 0.002)	4.0 ± 0.10 (0.157 ± 0.004)	2.5 (0.098)	8.3 (0.327)	Note 5
12mm	Single (4mm) & Double (8mm)	8.2 (0.323)	10.25 (0.404)	5.5 ± 0.05 (0.217 ± 0.002)	8.0 ± 0.10 (0.315 ± 0.004)	4.6 (0.181)	12.3 (0.484)	
16mm	Triple (12mm)	12.1 (0.476)	14.25 (0.561)	5.5 ± 0.05 (0.217 ± 0.002)	8.0 ± 0.10 (0.315 ± 0.004)	4.6 (0.181)	16.3 (0.642)	

1. The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.

2. The tape with or without components shall pass around R without damage (see Figure 5).

3. If S_1<1.0 mm, there may not be enough area for cover tape to be properly applied (see EIA Document 481 paragraph 4.3 (b)).

4. B1 dimension is a reference dimension for tape feeder clearance only.

5. The cavity defined by A_0, B_0 and K_0 shall surround the component with sufficient clearance that:

(a) the component does not protrude above the top surface of the carrier tape.

(b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.

(c) rotation of the component is limited to 20° maximum for 8 and 12mm tapes and 10° maximum for 16mm tapes (see Figure 3).

(d) lateral movement of the component is restricted to 0.5 mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16mm tape (see Figure 4)

(e) For KPS Series product A_0 and B_0 are measured on a plane 0.3mm above the bottom of the pocket.

(f) see Addendum in EIA Document 481 for standards relating to more precise taping requirements.

Figure 2 – Punched (Paper) Carrier Tape Dimensions

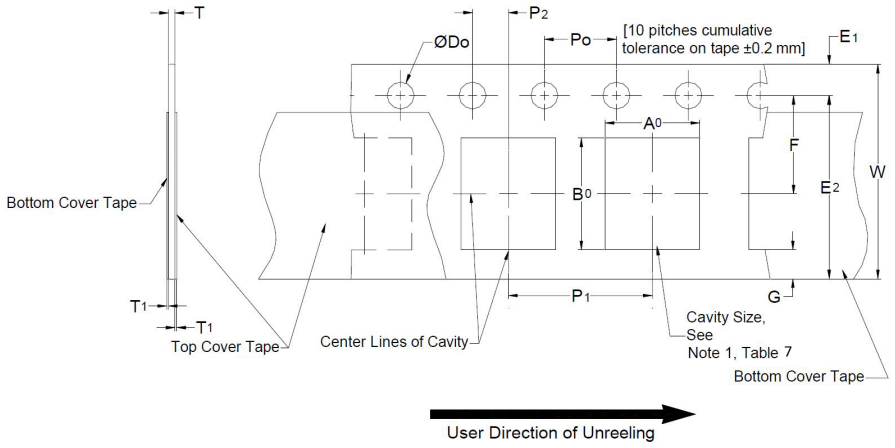


Table 7 - Punched (Paper) Carrier Tape Dimesions

(Metric will govern)

Constant Dimensions — Millimeters (Inches)							
Tape Size	D_0	E_1	P_0	P_2	T_1 Max	G Min	R Ref. Note 2
8mm	1.5 +0.10-0.0 (0.059 +0.004, -0.0)	1.75 ±0.10 (0.069 ±0.004)	4.0 ±0.10 (0.157 ±0.004)	2.0 ±0.05 (0.079 ±0.002)	0.10 (.004) Max.	0.75 (.030)	25 (.984)

Variable Dimensions — Millimeters (Inches)							
Tape Size	Pitch	E2 Min	F	P_1	T Max	W Max	A_0 B_0
8mm	Half (2mm)	6.25 (0.246)	3.5 ± 0.05 (0.138 ± 0.002)	2.0 ± 0.05 (0.079 ± 0.002)	1.1 (0.098)	8.3 (0.327)	Note 5
8mm	Single (4mm)			4.0 ± 0.10 (0.157 ± 0.004)		8.3 (0.327)	

1. The cavity defined by A_0, B_0 and T shall surround the component with sufficient clearance that:

a) the component does not protrude beyond either surface of the carrier tape.

b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.

d) lateral movement of the component is restricted to 0.5 mm maximum (see Figure 4).

e) see Addendum in EIA Document 481 for standards relating to more precise taping requirements.

2. The tape with or without components shall pass around R without damage (see Figure 5).

Packaging Information Performance Notes

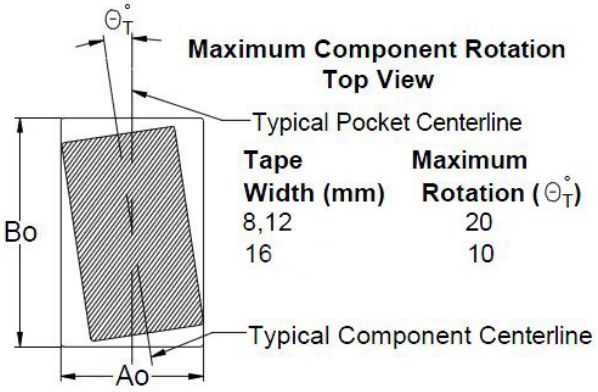
1. **Cover Tape Break Force:** *1.0 Kg Minimum.*
2. **Cover Tape Peel Strength:** *The total peel strength of the cover tape from the carrier tape shall be:*

Tape Width	Peel Strength
8mm	0.1 Newton to 1.0 Newton (10g to 100g)
12mm & 16mm	0.1 Newton to 1.3 Newton (10g to 130g)

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300±10 mm/minute.

3. **Labeling:** *Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. Refer to EIA-556 and EIA-624.*

Figure 3 – Maximum component rotation



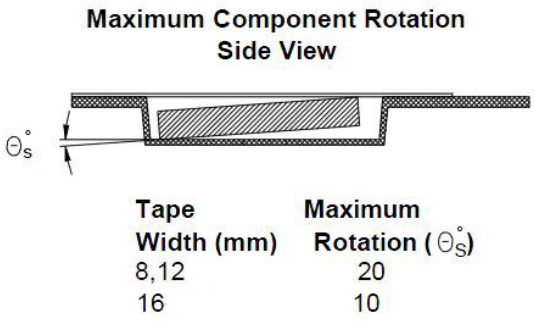


Figure 4 – Maximum lateral movement

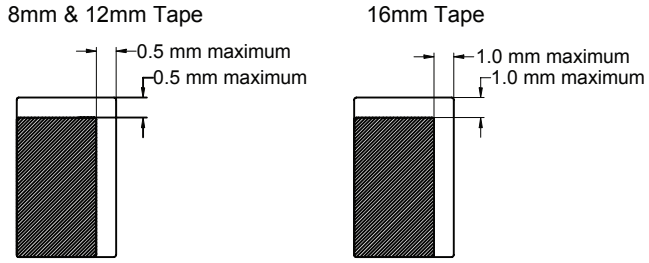


Figure 5 – Bending radius

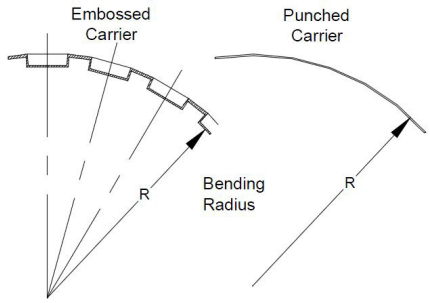
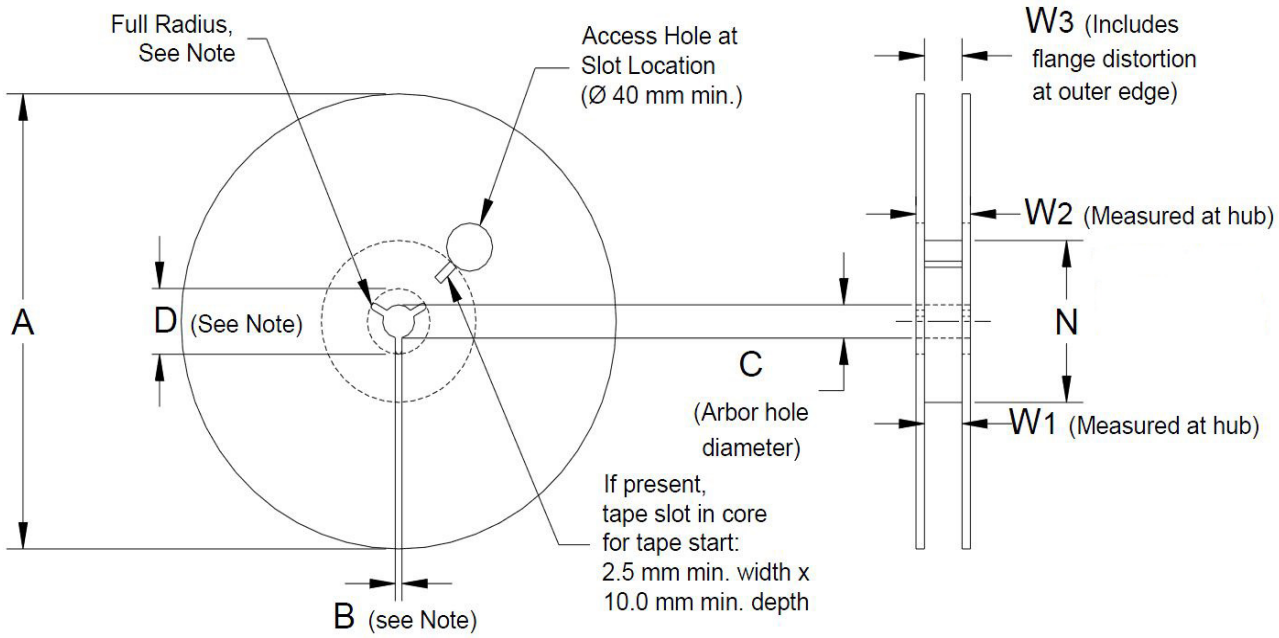


Figure 6 – Reel Dimensions



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Table 8 – Reel Dimensions

(Metric Dimensions Will Govern)

Constant Dimensions — Millimeters (Inches)				
Tape Size	A	B Min	C	D Min
8mm	178 ± 0.20 (7.008 ± 0.008) or 330 ± 0.20 (13.000 ± 0.008)	1.5 (0.059)	13.0 +0.5/-0.2 (0.521 +0.02/-0.008)	20.2 (0.795)
12mm				
16mm				

Variable Dimensions — Millimeters (Inches)				
Tape Size	N Min	W_1	W_2 Max	W_3
8mm	50 (1.969)	8.4 +1.5/-0.0 (0.331 +0.059/-0.0)	14.4 (0.567)	Shall Accommodate Tape Width Without Interference
12mm		12.4 +2.0/-0.0 (0.488 +0.078/-0.0)	18.4 (0.724)	
16mm		16.4 +2.0/-0.0 (0.646 +0.078/-0.0)	22.4 (0.882)	

Figure 7 – Tape leader & trailer dimensions

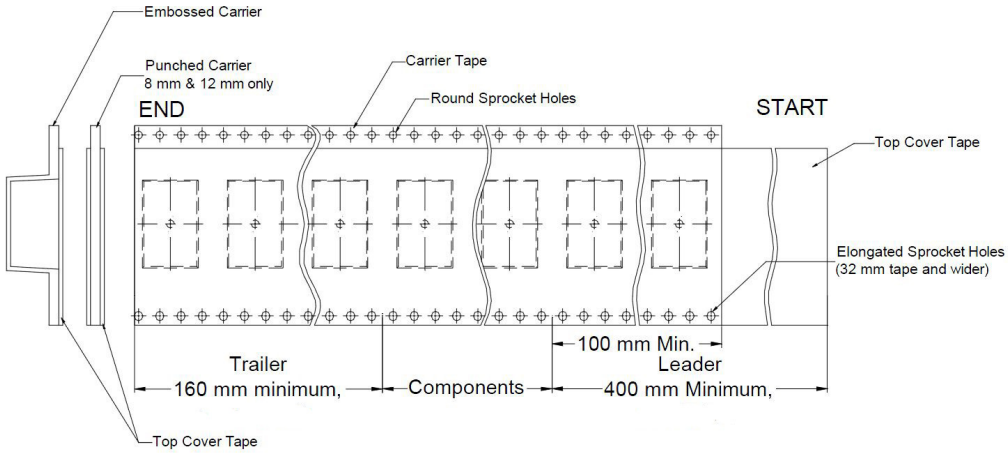
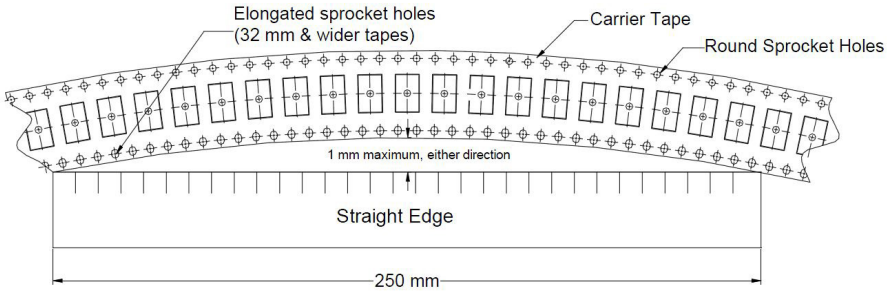


Figure 8 – Maximum camber



Other KEMET Resources

Tools	
Resource	Location
Configure A Part: CapEdge	http://capacitoredge.kemet.com
SPICE & FIT Software	http://www.kemet.com/spice
Search Our FAQs: KnowledgeEdge	http://www.kemet.com/keask

Product Information	
Resource	Location
Products	http://www.kemet.com/products
Technical Resources (Including Soldering Techniques)	http://www.kemet.com/technicalpapers
RoHS Statement	http://www.kemet.com/rohs
Quality Documents	http://www.kemet.com/qualitydocuments

Product Request	
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Engineering Kit Request	http://www.kemet.com/kits

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