

Multilayer ceramic capacitors are available in a variety of physical sizes and configurations, including leaded devices and surface mounted chips. Leaded styles include molded and conformally coated parts with axial and radial leads. However, the basic capacitor element is similar for all styles. It is called a chip and consists of formulated dielectric materials which have been cast into thin layers, interspersed with metal electrodes alternately exposed on opposite

edges of the laminated structure. The entire structure is fired at high temperature to produce a monolithic block which provides high capacitance values in a small physical volume. After firing, conductive terminations are applied to opposite ends of the chip to make contact with the exposed electrodes. Termination materials and methods vary depending on the intended use.

TEMPERATURE CHARACTERISTICS

Ceramic dielectric materials can be formulated with a wide range of characteristics. The EIA standard for ceramic dielectric capacitors (RS-198) divides ceramic dielectrics into the following classes:

Class I: Temperature compensating capacitors, suitable for resonant circuit application or other applications where high Q and stability of capacitance characteristics are required. Class I capacitors have predictable temperature coefficients and are not affected by voltage, frequency or time. They are made from materials which are not ferro-electric, yielding superior stability but low volumetric efficiency. Class I capacitors are the most stable type available, but have the lowest volumetric efficiency.

Class II: Stable capacitors, suitable for bypass or coupling applications or frequency discriminating circuits where Q and stability of capacitance characteristics are not of major importance. Class II capacitors have temperature characteristics of $\pm 15\%$ or less. They are made from materials which are ferro-electric, yielding higher volumetric efficiency but less stability. Class II capacitors are affected by temperature, voltage, frequency and time.

Class III: General purpose capacitors, suitable for by-pass coupling or other applications in which dielectric losses, high insulation resistance and stability of capacitance characteristics are of little or no importance. Class III capacitors are similar to Class II capacitors except for temperature characteristics, which are greater than $\pm 15\%$. Class III capacitors have the highest volumetric efficiency and poorest stability of any type.

KEMET leaded ceramic capacitors are offered in the three most popular temperature characteristics:

C0G: Class I, with a temperature coefficient of 0 ± 30 ppm per degree C over an operating temperature range of -55°C to $+125^{\circ}\text{C}$ (Also known as "NP0").

X7R: Class II, with a maximum capacitance change of $\pm 15\%$ over an operating temperature range of -55°C to $+125^{\circ}\text{C}$.

Z5U: Class III, with a maximum capacitance change of $+22\% - 56\%$ over an operating temperature range of $+10^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Specified electrical limits for these three temperature characteristics are shown in Table 1.

SPECIFIED ELECTRICAL LIMITS

Parameter	Temperature Characteristics		
	C0G	X7R	Z5U
Dissipation Factor: Measured at following conditions. C0G – 1 kHz and 1 vrms if capacitance $>1000\text{pF}$ 1 MHz and 1 vrms if capacitance $\leq 1000\text{ pF}$ X7R – 1 kHz and 1 vrms* or if extended cap range 0.5 vrms Z5U – 1 kHz and 0.5 vrms	0.10%	2.5% (3.5% @ 25V)	4.0%
Dielectric Strength: 2.5 times rated DC voltage.	Pass Subsequent IR Test		
Insulation Resistance (IR): At rated DC voltage, whichever of the two is smaller	1,000 M Ω - μF or 100 G Ω	1,000 M Ω - μF or 100 G Ω	1,000 M Ω - μF or 10 G Ω
Temperature Characteristics: Range, $^{\circ}\text{C}$ Capacitance Change without DC voltage	-55 to +125 $0 \pm 30\text{ ppm}/^{\circ}\text{C}$	-55 to +125 $\pm 15\%$	+ 10 to +85 $+22\%, -56\%$

* MHz and 1 vrms if capacitance $\leq 100\text{ pF}$ on military product.

Table I

APPLICATION NOTES FOR MULTILAYER CERAMIC CAPACITORS

ELECTRICAL CHARACTERISTICS

The fundamental electrical properties of multilayer ceramic capacitors are as follows:

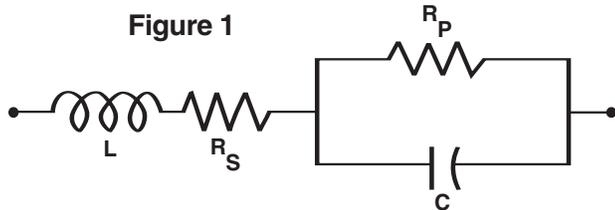
Polarity: Multilayer ceramic capacitors are not polar, and may be used with DC voltage applied in either direction.

Rated Voltage: This term refers to the maximum continuous DC working voltage permissible across the entire operating temperature range. Multilayer ceramic capacitors are not extremely sensitive to voltage, and brief applications of voltage above rated will not result in immediate failure. However, reliability will be reduced by exposure to sustained voltages above rated.

Capacitance: The standard unit of capacitance is the farad. For practical capacitors, it is usually expressed in microfarads (10^{-6} farad), nanofarads (10^{-9} farad), or picofarads (10^{-12} farad). Standard measurement conditions are as follows:

Class I (up to 1,000 pF):	1MHz and 1.2 VRMS maximum.
Class I (over 1,000 pF):	1kHz and 1.2 VRMS maximum.
Class II:	1 kHz and 1.0 ± 0.2 VRMS.
Class III:	1 kHz and 0.5 ± 0.1 VRMS.

Like all other practical capacitors, multilayer ceramic capacitors also have resistance and inductance. A simplified schematic for the equivalent circuit is shown in Figure 1. Other significant electrical characteristics resulting from these additional properties are as follows:



C = Capacitance **RS = Equivalent Series Resistance (ESR)**
L = Inductance **RP = Insulation Resistance (IR)**

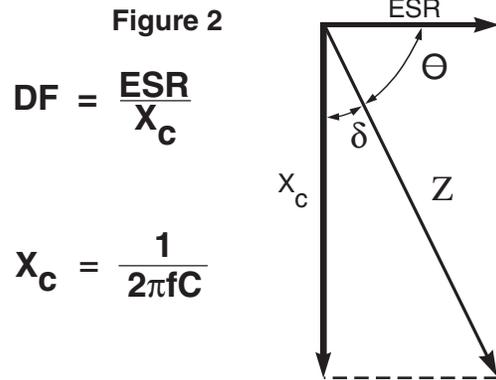
Impedance: Since the parallel resistance (Rp) is normally very high, the total impedance of the capacitor is:

$$Z = \sqrt{R_S^2 + (X_C - X_L)^2}$$

Where **Z = Total Impedance**
RS = Equivalent Series Resistance
XC = Capacitive Reactance = $\frac{1}{2\pi fC}$
XL = Inductive Reactance = $2\pi fL$

The variation of a capacitor's impedance with frequency determines its effectiveness in many applications.

Dissipation Factor: Dissipation Factor (DF) is a measure of the losses in a capacitor under AC application. It is the ratio of the equivalent series resistance to the capacitive reactance, and is usually expressed in percent. It is usually measured simultaneously with capacitance, and under the same conditions. The vector diagram in Figure 2 illustrates the relationship between DF, ESR, and impedance. The reciprocal of the dissipation factor is called the "Q", or quality factor. For convenience, the "Q" factor is often used for very low values of dissipation factor. DF is sometimes called the "loss tangent" or "tangent δ ", as derived from this diagram.



$$DF = \frac{ESR}{X_C}$$

$$X_C = \frac{1}{2\pi fC}$$

Insulation Resistance: Insulation Resistance (IR) is the DC resistance measured across the terminals of a capacitor, represented by the parallel resistance (Rp) shown in Figure 1. For a given dielectric type, electrode area increases with capacitance, resulting in a decrease in the insulation resistance. Consequently, insulation resistance is usually specified as the "RC" (IR x C) product, in terms of ohm-farads or megohm-microfarads. The insulation resistance for a specific capacitance value is determined by dividing this product by the capacitance. However, as the nominal capacitance values become small, the insulation resistance calculated from the RC product reaches values which are impractical. Consequently, IR specifications usually include both a minimum RC product and a maximum limit on the IR calculated from that value. For example, a typical IR specification might read "1,000 megohm-microfarads or 100 gigohms, whichever is less."

Insulation Resistance is the measure of a capacitor to resist the flow of DC leakage current. It is sometimes referred to as "leakage resistance." The DC leakage current may be calculated by dividing the applied voltage by the insulation resistance (Ohm's Law).

Dielectric Withstanding Voltage: Dielectric withstanding voltage (DWV) is the peak voltage which a capacitor is designed to withstand for short periods of time without damage. All KEMET multilayer ceramic capacitors will withstand a test voltage of 2.5 x the rated voltage for 60 seconds.

KEMET specification limits for these characteristics at standard measurement conditions are shown in Table 1 on page 4. Variations in these properties caused by changing conditions of temperature, voltage, frequency, and time are covered in the following sections.

TABLE 1
EIA TEMPERATURE CHARACTERISTIC CODES
FOR CLASS I DIELECTRICS

Significant Figure of Temperature Coefficient		Multiplier Applied to Temperature Coefficient		Tolerance of Temperature Coefficient *	
PPM per Degree C	Letter Symbol	Multiplier	Number Symbol	PPM per Degree C	Letter Symbol
0.0	C	-1	0	±30	G
0.3	B	-10	1	±60	H
0.9	A	-100	2	±120	J
1.0	M	-1000	3	±250	K
1.5	P	-100000	4	±500	L
2.2	R	+1	5	±1000	M
3.3	S	+10	6	±2500	N
4.7	T	+100	7		
7.5	U	+1000	8		
		+10000	9		

* These symmetrical tolerances apply to a two-point measurement of temperature coefficient: one at 25°C and one at 85°C. Some deviation is permitted at lower temperatures. For example, the PPM tolerance for C0G at -55°C is +30 / -72 PPM.

TABLE 2
EIA TEMPERATURE CHARACTERISTIC CODES
FOR CLASS II & III DIELECTRICS

Low Temperature Rating		High Temperature Rating		Maximum Capacitance Shift	
Degree Celcius	Letter Symbol	Degree Celcius	Number Symbol	Percent	Letter Symbol
+10C	Z	+45C	2	±1.0%	A
-30C	Y	+65C	4	±1.5%	B
-55C	X	+85C	5	±2.2%	C
		+105C	6	±3.3%	D
		+125C	7	±4.7%	E
		+150C	8	±7.5%	F
		+200C	9	±10.0%	P
				±15.0%	R
				±22.0%	S
				+22/-33%	T
				+22/-56%	U
				+22/-82%	V

EFFECT OF TEMPERATURE

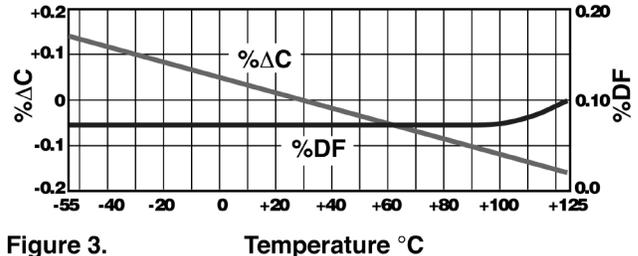


Figure 3. Temperature °C
Capacitance & DF vs Temperature - C0G

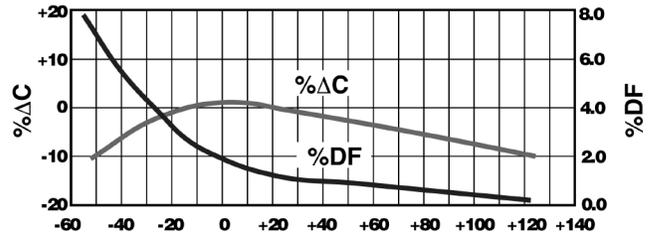


Figure 4. Temperature °C
Capacitance & DF vs Temperature - X7R

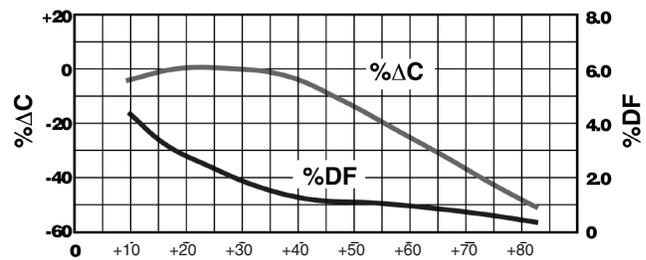


Figure 5. Temperature °C
Capacitance & DF vs Temperature - Z5U

APPLICATION NOTES FOR MULTILAYER CERAMIC CAPACITORS

EFFECT OF APPLIED VOLTAGE

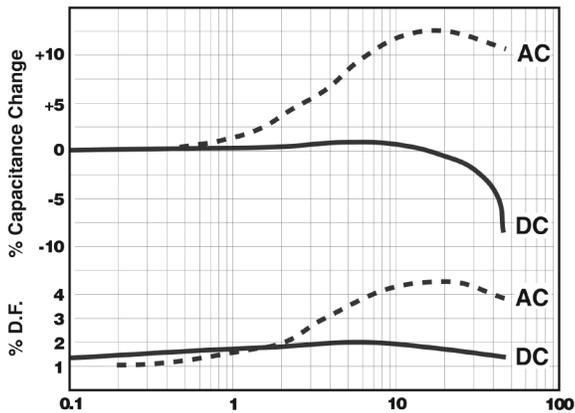


Figure 6. AC or DC Volts Applied
Typical Effects of 1000 Hz AC and DC Voltage Level on Capacitance and Dissipation Factor - X7R

Note: COG Dielectric capacitance and dissipation factor are stable with voltage.

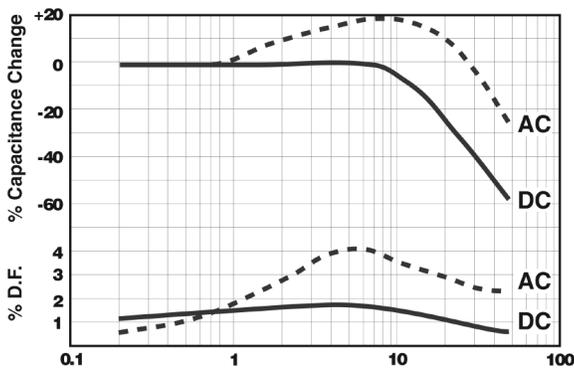


Figure 7. AC or DC Volts Applied
Typical Effects of 1000 Hz AC and DC Voltage Level on Capacitance and Dissipation Factor - Z5U

Note: COG Dielectric capacitance and dissipation factor are stable with voltage.

Effect of Temperature: Both capacitance and dissipation factor are affected by variations in temperature. The maximum capacitance change with temperature is defined by the temperature characteristic. However, this only defines a “box” bounded by the upper and lower operating temperatures and the minimum and maximum capacitance values. Within this “box”, the variation with temperature depends upon the specific dielectric formulation. Typical curves for KEMET capacitors are shown in Figures 3, 4, and 5. These figures also include the typical change in dissipation factor for KEMET capacitors.

Insulation resistance decreases with temperature. Typically, the insulation resistance at maximum rated temperature is 10% of the 25°C value.

Effect of Voltage: Class I ceramic capacitors are not affected by variations in applied AC or DC voltages. For Class II and III ceramic capacitors, variations in voltage affect only the capacitance and dissipation factor. The application of DC voltage higher than 5 vdc reduces both the capacitance and dissipation factor. The application of AC voltages up to 10-20 Vac tends to increase both capacitance and dissipation factor.

At higher AC voltages, both capacitance and dissipation factor begin to decrease.

Typical curves showing the effect of applied AC and DC voltage are shown in Figure 6 for KEMET X7R capacitors and Figure 7 for KEMET Z5U capacitors.

Effect of Frequency: Frequency affects both capacitance and dissipation factor. Typical curves for KEMET multilayer ceramic capacitors are shown in Figures 8 and 9.

The variation of impedance with frequency is an important consideration in the application of multilayer ceramic capacitors. Total impedance of the capacitor is the vector of the capacitive reactance, the inductive reactance, and the ESR, as illustrated in Figure 2. As frequency increases, the capacitive reactance decreases. However, the series inductance (L) shown in Figure 1 produces inductive reactance, which increases with frequency. At some frequency, the impedance ceases to be capacitive and becomes inductive. This point, at the bottom of the V-shaped impedance versus frequency curves, is the self-resonant frequency. At the self-resonant frequency, the reactance is zero, and the impedance consists of the ESR only.

Typical impedance versus frequency curves for KEMET multilayer ceramic capacitors are shown in Figures 10, 11, and 12. These curves apply to KEMET capacitors in chip form, without leads. Lead configuration and lead length have a significant impact on the series inductance. The lead inductance is approximately 10nH/inch, which is large compared to the inductance of the chip. The effect of this additional inductance is a decrease in the self-resonant frequency, and an increase in impedance in the inductive region above the self-resonant frequency.

Effect of Time: The capacitance of Class II and III dielectrics change with time as well as with temperature, voltage and frequency. This change with time is known as “aging.” It is caused by gradual realignment of the crystalline structure of the ceramic dielectric material as it is cooled below its Curie temperature, which produces a loss of capacitance with time. The aging process is predictable and follows a logarithmic decay. Typical aging rates for COG, X7R, and Z5U dielectrics are as follows:

COG	None
X7R	2.0% per decade of time
Z5U	5.0% per decade of time

Typical aging curves for X7R and Z5U dielectrics are shown in Figure 13.

The aging process is reversible. If the capacitor is heated to a temperature above its Curie point for some period of time, de-aging will occur and the capacitor will regain the capacitance lost during the aging process. The amount of de-aging depends on both the elevated temperature and the length of time at that temperature. Exposure to 150°C for one-half hour or 125°C for two hours is usually sufficient to return the capacitor to its initial value.

Because the capacitance changes rapidly immediately after de-aging, capacitance measurements are usually delayed for at least 10 hours after the de-aging process, which is often referred to as the “last heat.” In addition, manufacturers utilize the aging rates to set factory test limits which will bring the capacitance within the specified tolerance at some future time, to allow for customer receipt and use. Typically, the test limits are adjusted so that the capacitance will be within the specified tolerance after either 1,000 hours or 100 days, depending on the manufacturer and the product type.

POWER DISSIPATION

Power dissipation has been empirically determined for two representative KEMET series: C052 and C062. Power dissipation capability for various mounting configurations is shown in Table 3. This table was extracted from Engineering Bulletin F-2013, which provides a more detailed treatment of this subject.

Note that no significant difference was detected between the two sizes in spite of a 2 to 1 surface area ratio. Due to the materials used in the construction of multilayer ceramic capacitors, the power dissipation capability does not depend greatly on the surface area of the capacitor body, but rather on how well heat is conducted out of the capacitor lead wires. Consequently, this power dissipation capability is applicable to other leaded multilayer styles and sizes.

TABLE 3
POWER DISSIPATION CAPABILITY
(Rise in Celsius degrees per Watt)

Mounting Configuration	Power Dissipation of C052 & C062
1.00" leadwires attached to binding post of GR-1615 bridge (excellent heat sink)	90 Celsius degrees rise per Watt ±10%
0.25" leadwires attached to binding post of GR-1615 bridge	55 Celsius degrees rise per Watt ±10%
Capacitor mounted flush to 0.062" glass-epoxy circuit board with small copper traces	77 Celsius degrees rise per Watt ±10%
Capacitor mounted flush to 0.062" glass-epoxy circuit board with four square inches of copper land area as a heat sink	53 Celsius degrees rise per Watt ±10%

As shown in Table 3, the power dissipation capability of the capacitor is very sensitive to the details of its use environment. The temperature rise due to power dissipation should not exceed 20°C. Using that constraint, the maximum permissible power dissipation may be calculated from the data provided in Table 3.

It is often convenient to translate power dissipation capability into a permissible AC voltage rating. Assuming a sinusoidal wave form, the RMS "ripple voltage" may be calculated from the following formula:

$$E = Z \times \sqrt{\frac{P_{MAX}}{R}}$$

Where **E = RMS Ripple Voltage (volts)**

P = Power Dissipation (watts)

Z = Impedance

R = ESR

The data necessary to make this calculation is included in Engineering Bulletin F-2013. However, the following criteria must be observed:

1. The temperature rise due to power dissipation should be limited to 20°C.
2. The peak AC voltage plus the DC voltage must not exceed the maximum working voltage of the capacitor.

Provided that these criteria are met, multilayer ceramic

capacitors may be operated with AC voltage applied without need for DC bias.

RELIABILITY

A well constructed multilayer ceramic capacitor is extremely reliable and, for all practical purposes, has an infinite life span when used within the maximum voltage and temperature ratings. Capacitor failure may be induced by sustained operation at voltages that exceed the rated DC voltage, voltage spikes or transients that exceed the dielectric withstanding voltage, sustained operation at temperatures above the maximum rated temperature, or the excessive temperature rise due to power dissipation.

Failure rate is usually expressed in terms of percent per 1,000 hours or in FITS (failure per billion hours). Some KEMET series are qualified under U.S. military established reliability specifications MIL-PRF-20, MIL-PRF-123, MIL-PRF-39014, and MIL-PRF-55681. Failure rates as low as 0.001% per 1,000 hours are available for all capacitance / voltage ratings covered by these specifications. These specifications and accompanying Qualified Products List should be consulted for details.

For series not covered by these military specifications, an internal testing program is maintained by KEMET Quality Assurance. Samples from each week's production are subjected to a 2,000 hour accelerated life test at 2 x rated voltage and maximum rated temperature. Based on the results of these tests, the average failure rate for all non-military series covered by this test program is currently 0.06% per 1,000 hours at maximum rated conditions. The failure rate would be much lower at typical use conditions. For example, using MIL-HDBK-217D this failure rate translates to 0.9 FITS at 50% rated voltage and 50°C.

Current failure rate details for specific KEMET multilayer ceramic capacitor series are available on request.

MISAPPLICATION

Ceramic capacitors, like any other capacitors, may fail if they are misapplied. Typical misapplications include exposure to excessive voltage, current or temperature. If the dielectric layer of the capacitor is damaged by misapplication the electrical energy of the circuit can be released as heat, which may damage the circuit board and other components as well.

If potential for misapplication exists, it is recommended that precautions be taken to protect personnel and equipment during initial application of voltage. Commonly used precautions include shielding of personnel and sensing for excessive power drain during board testing.

STORAGE AND HANDLING

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature – reels may soften or warp, and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40° C, and maximum storage humidity not exceed 70% relative humidity. In addition, temperature fluctuations should be minimized to avoid condensation on the parts, and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability, chip stock should be used promptly, preferably within 1.5 years of receipt.

APPLICATION NOTES FOR MULTILAYER CERAMIC CAPACITORS

EFFECT OF FREQUENCY

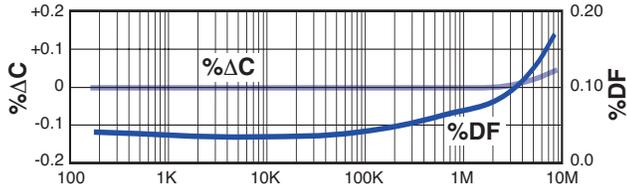


Figure 8. Frequency - Hertz
Capacitance & DF vs Frequency - C0G

IMPEDANCE VS FREQUENCY

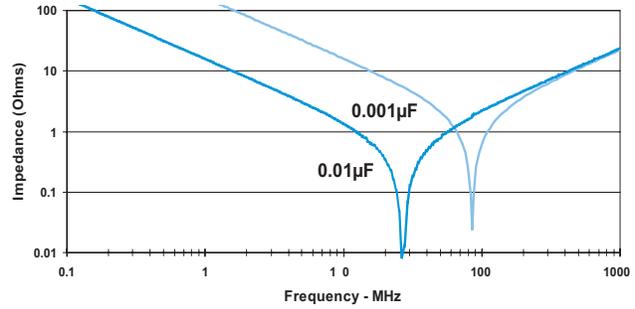


Figure 10. Impedance vs Frequency
for C0G Dielectric

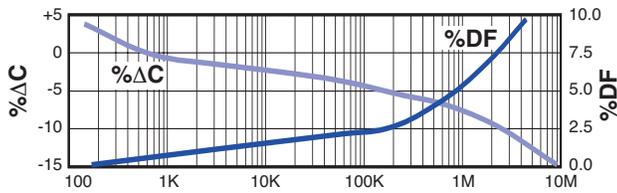


Figure 9. Frequency - Hertz
Capacitance & DF vs Frequency - X7R & Z5U

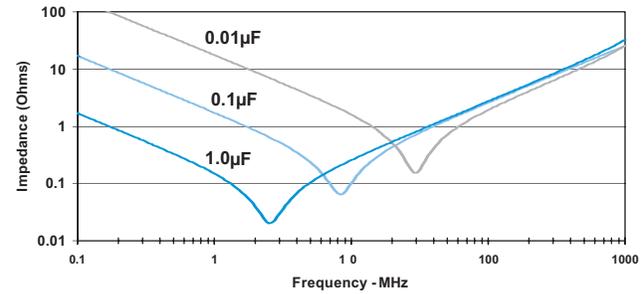


Figure 11. Impedance vs Frequency
for X7R Dielectric

EFFECT OF TIME (hours)

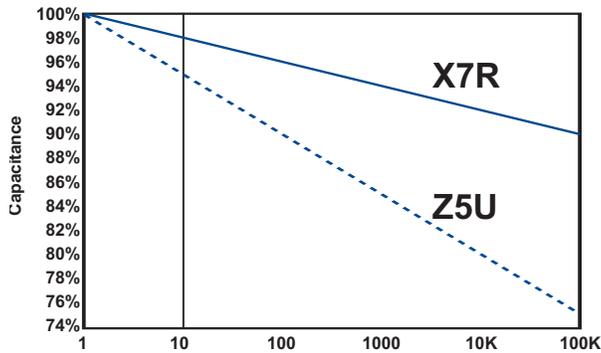


Figure 13. Typical Aging Rates for X7R & Z5U

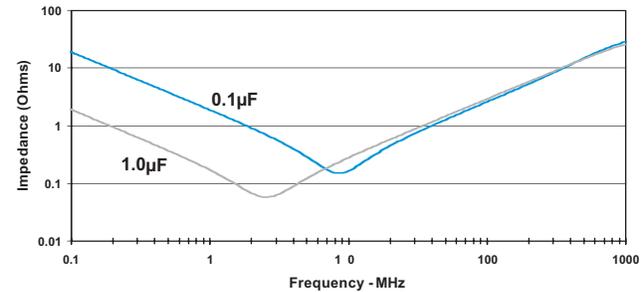


Figure 12. Impedance vs Frequency
for Z5U Dielectric

GENERAL SPECIFICATIONS**Working Voltage:****Axial (WVDC)**

C0G 50, 100, 200
X7R 25, 50, 100, 200, 250
Z5U 50, 100

Radial (WVDC)

C0G 50, 100, 200, 500, 1k, 1.5k, 2k, 2.5k, 3k
X7R 25, 50, 100, 200, 250, 500, 1k, 1.5k, 2k, 2.5k, 3k
Z5U 50, 100

Temperature Characteristics:

C0G 0 ±30 PPM / °C from -55°C to +125°C (1)
X7R ± 15% from -55°C to +125°C
Z5U + 22%, -56% from +10°C to +85°C

Capacitance Tolerance:

C0G ±0.5pF, ±1%, ±2%, ±5%, ±10%, ±20%
X7R ±10%, ±20%, +80% / -20%
Z5U ±20%, 80% / -20%

Construction:

Epoxy encapsulated – meets flame test requirements of UL Standard 94V-0.

High-temperature solder – meets EIA RS-198, Method 302, Condition B (260°C for 10 seconds)

Lead Material:

Standard: 100% matte tin (Sn) with nickel (Ni) underplate and steel core ("TA" designation).

Alternative 1: 60% Tin (Sn)/40% Lead (Pb) finish with copper-clad steel core ("HA" designation).

Alternative 2: 60% Tin (Sn)/40% Lead (Pb) finish with 100% copper core (available with "HA" termination code with c-spec)

Solderability:

EIA RS-198, Method 301, Solder Temperature: 230°C ±5°C.
Dwell time in solder = 7 ± ½ seconds.

Terminal Strength:

EIA RS-198, Method 303, Condition A (2.2kg)

ELECTRICAL**Capacitance @ 25°C:**

Within specified tolerance and following test conditions.

C0G – >1000pF with 1.0 vrms @ 1 kHz

≤ 1000pF with 1.0 vrms @ 1 MHz

X7R – with 1.0 vrms @ 1 kHz (Referee Time: 1,000 hours)

Z5U – with 1.0 vrms @ 1 kHz

Dissipation Factor @25°C:

Same test conditions as capacitance.

C0G – 0.10% maximum

X7R – 2.5% maximum (3.5% for 25V)

Z5U – 4.0% maximum

Insulation Resistance @25°C:

EIA RS-198, Method 104, Condition A <1kV

C0G – 100 GΩ or 1000 MΩ – μF, whichever is less.

≤500V test @ rated voltage, >500V test @ 500V

X7R – 100 GΩ or 1000 MΩ – μF, whichever is less.

≤500V test @ rated voltage, >500V test @ 500V

Z5U – 10 GΩ or 1000 MΩ – μF, whichever is less.

Dielectric Withstanding Voltage:

EIA RS-198, Method 103

≤250V test @ 250% of rated voltage for 5 seconds
with current limited to 50mA.

500V test @ 150% of rated voltage for 5 seconds
with current limited to 50mA.

≥1000V test @ 120% of rated voltage for 5 seconds
with current limited to 50mA.

ENVIRONMENTAL**Vibration:**

EIA RS-198, Method 304, Condition D (10-2000Hz; 20g)

Shock:

EIA RS-198, Method 305, Condition I (100g)

Life Test:

EIA RS-198, Method 201, Condition D.

<200V

C0G – 200% of rated voltage @ +125°C

X7R – 200% of rated voltage @ +125°C

Z5U – 200% of rated voltage @ +85°C

>500V

C0G – rated voltage @ +125°C

X7R – rated voltage @ +125°C

Post Test Limits @ 25°C are:**Capacitance Change:**

C0G (≤ 200V) – ±3% or 0.25pF, whichever is greater.

C0G (≥ 500V) – ±3% or 0.50pF, whichever is greater.

X7R – ± 20% of initial value (2)

Z5U – ± 30% of initial value (2)

Dissipation Factor:

C0G – 0.10% maximum

X7R – 2.5% maximum (3.5% for 25V)

Z5U – 4.0% maximum

Insulation Resistance:

C0G – 10 GΩ or 100 MΩ – μF, whichever is less.

>1kV tested @ 500V.

X7R – 10 GΩ or 100 MΩ – μF, whichever is less.

>1kV tested @ 500V.

Z5U – 1 GΩ or 100 MΩ – μF, whichever is less.

Moisture Resistance:

EIA RS-198, Method 204, Condition A (10 cycles without applied voltage).

Post Test Limits @ 25°C are:**Capacitance Change:**

C0G (≤ 200V) – ±3% or ±0.25pF, whichever is greater.

C0G (≥ 500V) – ±3% or ± 0.50pF, whichever is greater.

X7R – ± 20% of initial value (2)

Z5U – ± 30% of initial value (2)

Dissipation Factor:

C0G – 0.10% maximum

X7R – 2.5% maximum (3.5% for 25V)

Z5U – 4.0% maximum

Insulation Resistance:

C0G – 10 GΩ or 100 MΩ – μF whichever is less.

≤500V test @ rated voltage, >500V test @ 500V.

X7R – 10 GΩ or 100 MΩ – μF, whichever is less.

≤500V test @ rated voltage, >500V test @ 500V.

Z5U – 1k MΩ or 100 MΩ – μF, whichever is less.

Thermal Shock:

EIA RS-198, Method 202, Condition B (C0G & X7R: -55°C to 125°C); Condition A (Z5U: -55°C to 85°C)

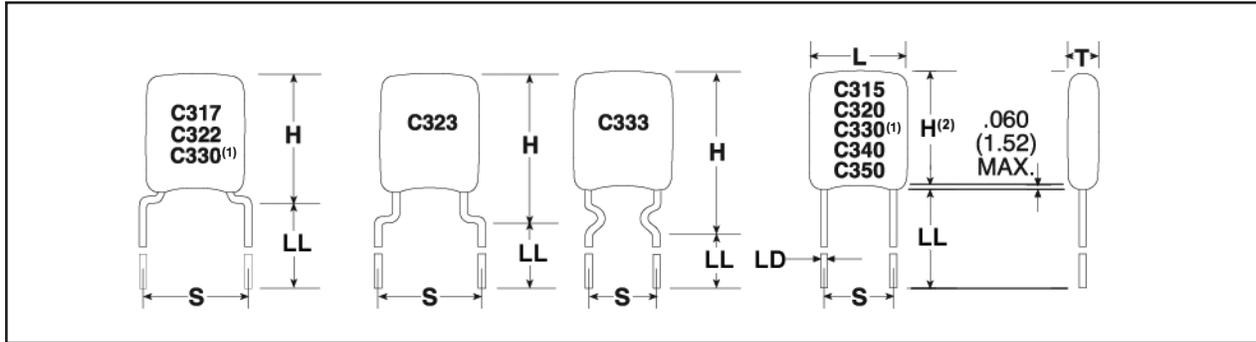
(1) +53 PPM -30 PPM/ °C from +25°C to -55°C, + 60 PPM below 10pF.

(2) X7R and Z5U dielectrics exhibit aging characteristics; therefore, it is highly recommended that capacitors be deaged for 2 hours at 150°C and stabilized at room temperature for 48 hours before capacitance measurements are made.

CERAMIC CONFORMALLY COATED/RADIAL

"STANDARD & HIGH VOLTAGE GOLD MAX"

STANDARD LEAD CONFIGURATION OUTLINE DRAWINGS



Drawings are not to scale. See table below for dimensions. See page 16 for optional lead configurations.

(1) Lead configuration depends on capacitance value. (2) H dimensions does not include meniscus.

DIMENSIONS INCHES (MILLIMETERS)

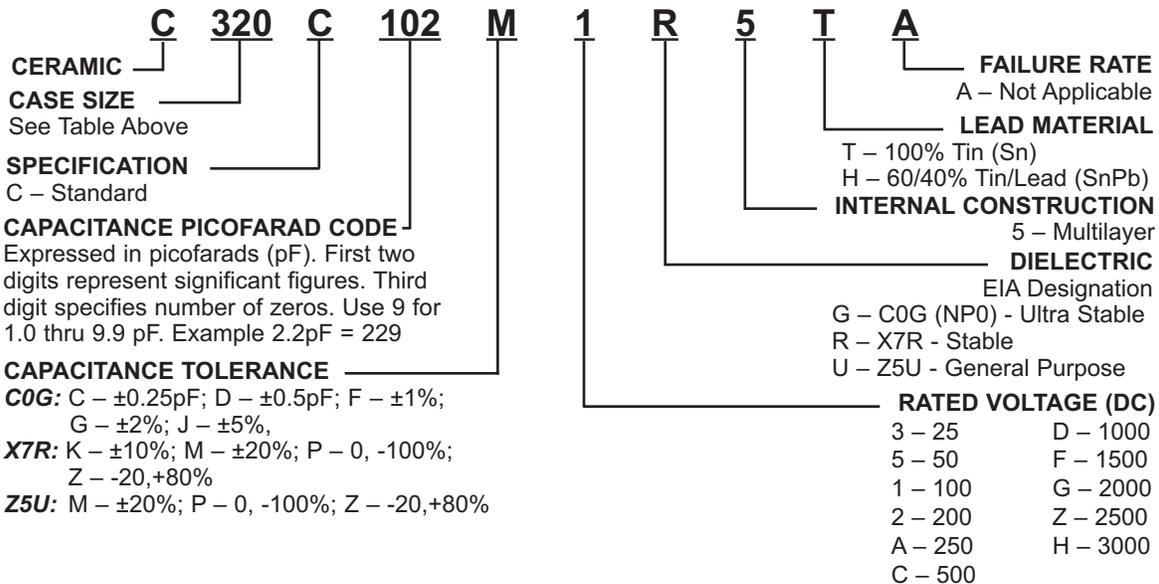
Case Size	L Max.	H. Max.	Standard T Max.	High Voltage T Max.	S ⁽¹⁾ ±.030 (.78)	LD +.004(.10) -.001(.025)	LL Min.
C315	0.150 (3.81)	0.210 (5.33)	0.100 (2.54)	0.150 (3.81)	0.100 (2.54)	0.020 (.51)	0.276 (7.00)
C317	0.150 (3.81)	0.230 (5.84)	0.100 (2.54)	0.150 (3.81)	0.200 (5.08)	0.020 (.51)	0.276 (7.00)
C320	0.200 (5.08)	0.260 (6.60)	0.125 (3.18) ⁽²⁾	0.200 (5.08)	0.100 (2.54)	0.020 (.51)	0.276 (7.00)
C322	0.200 (5.08)	0.260 (6.60)	0.125 (3.18)	0.200 (5.08)	0.200 (5.08)	0.020 (.51)	0.276 (7.00)
C323	0.200 (5.08)	0.320 (8.13)	0.125 (3.18)	0.200 (5.08)	0.200 (5.08)	0.020 (.51)	0.276 (7.00)
C330	0.300 (7.62)	0.360 (9.14)	0.150 (3.81)	0.250 (6.35)	0.200 (5.08)	0.020 (.51)	0.276 (7.00)
C333	0.300 (7.62)	0.390 (9.91)	0.150 (3.81)	0.250 (6.35)	0.200 (5.08)	0.020 (.51)	0.276 (7.00)
C340	0.400 (10.16)	0.460 (11.68)	0.150 (3.81)	0.270 (6.86)	0.200 (5.08)	0.020 (.51)	0.276 (7.00)
C350	0.500 (12.70)	0.560 (14.22)	0.200 (5.08)	0.270 (6.86)	0.400 (10.16)	0.025 (.64)	0.276 (7.00)

Note: 1 inch = 25.4mm.

Note (1): Measured at seating plane.

Note (2): Thickness = 0.16" (4.064mm) for C320 from 4.7 - 10.0µF.

ORDERING INFORMATION



For packaging information, see pages 47 and 48.

OPTIONAL CONFIGURATIONS BY LEAD SPACING

The preferred lead wire configurations are shown on page 15. However, additional configurations are available. All available options, including those on page 15, are shown below grouped by lead spacing.

Lead Spacing .100" ± .030	C 3 1 5 	C 3 1 6 	C 3 2 0 	C 3 2 4 	C 3 2 6
	Lead Spacing .200" ± .030	C 3 1 7 	C 3 1 8 	C 3 2 2 	C 3 2 3
Lead Spacing .200" ± .030	C 3 2 5 	C 3 2 7 	C 3 2 8 		
Lead Spacing .200" ± .030 Note: C330 configuration depends on capacitance. See part number tables for specifics.	C 3 3 0 	C 3 3 3 	C 3 3 5 	C 3 3 6 	C 3 4 0
	C 3 4 6 				
Lead Spacing .250" ± .030 (Available in bulk only)	C 3 2 1 	C 3 3 1 	Lead Spacing .400" ± .030		C 3 5 0
					C 3 5 6

Note: Non-standard lead lengths are available in bulk only.

CERAMIC CONFORMALLY COATED/RADIAL

"STANDARD & HIGH VOLTAGE GOLD MAX"

RATINGS & PART NUMBER REFERENCE

GENERAL PURPOSE TEMPERATURE CHARACTERISTIC — Z5U

		Style	C31X			C32X			C33X			C34X			C35X		
Cap	Cap Code	Cap Tol	WVDC			WVDC			WVDC			WVDC			WVDC		
			50	100	200	50	100	200	50	100	200	50	100	200	50	100	200
1000pF	102	M,P,Z															
1200	122	M,P,Z															
1500	152	M,P,Z															
1800	182	M,P,Z															
2200	222	M,P,Z															
2700	272	M,P,Z															
3300	332	M,P,Z															
3900	392	M,P,Z															
4700	472	M,P,Z															
5600	562	M,P,Z															
6800	682	M,P,Z															
8200	822	M,P,Z															
.010uF	103	M,P,Z															
.012	123	M,P,Z															
.015	153	M,P,Z															
.018	183	M,P,Z															
.022	223	M,P,Z															
.027	273	M,P,Z															
.033	333	M,P,Z															
.039	393	M,P,Z															
.047	473	M,P,Z															
.056	563	M,P,Z															
.068	683	M,P,Z															
.082	823	M,P,Z															
.10	104	M,P,Z															
.12	124	M,P,Z															
.15	154	M,P,Z															
.18	184	M,P,Z															
.22	224	M,P,Z															
.27	274	M,P,Z															
.33	334	M,P,Z															
.39	394	M,P,Z															
.47	474	M,P,Z															
.56	564	M,P,Z															
.68	684	M,P,Z															
.82	824	M,P,Z															
1.0	105	M,P,Z															
1.2	125	M,P,Z															
1.5	155	M,P,Z															
1.8	185	M,P,Z															
2.2	225	M,P,Z															
2.7	275	M,P,Z															
3.3	335	M,P,Z															
3.9	395	M,P,Z															
4.7	475	M,P,Z															
5.6	565	M,P,Z															
6.8	685	M,P,Z															
1	Requires straight leads (all other C33x's require bent leads)																

For packaging information, see pages 47 and 48.

Gold Max

CERAMIC LEADED PACKAGING INFORMATION

Ceramic Radial Lead Tape and Reel Packaging

KEMET offers standard reeling of Molded and Conformally Coated Radial Leaded Ceramic Capacitors for automatic insertion per EIA specification RS-468. Parts are taped to a tagboard carrier strip, and wound on a reel as shown in Figure 1. Kraft paper interleaving is inserted between the layers of capacitors on the reel. Ammopack is also available, with the same lead tape configuration and package quantities.

Figure 1

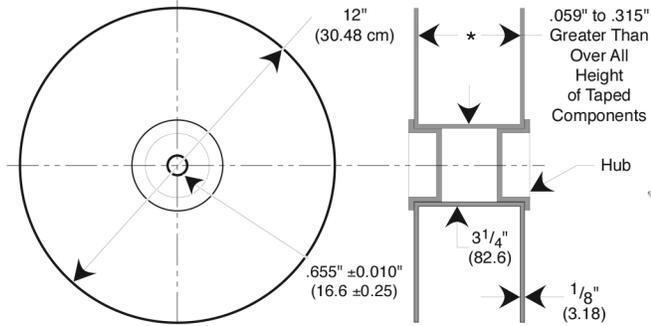
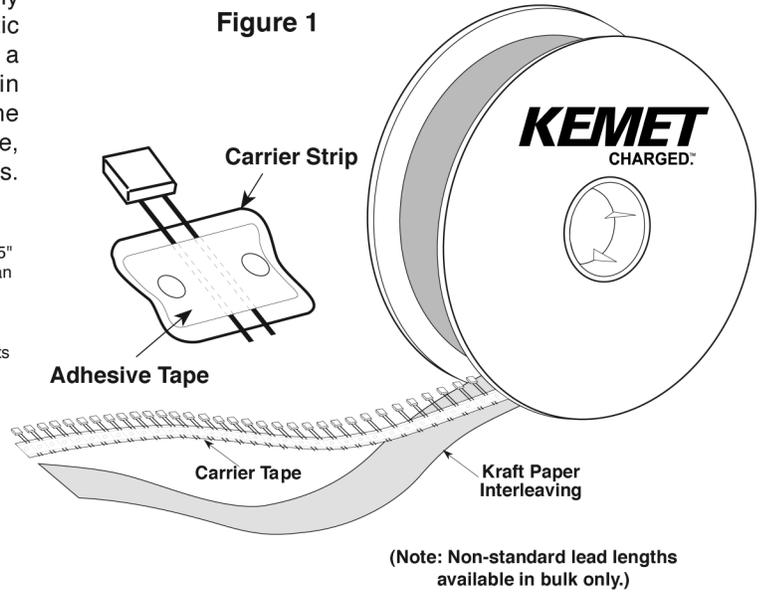


Figure 3: Standard Reel

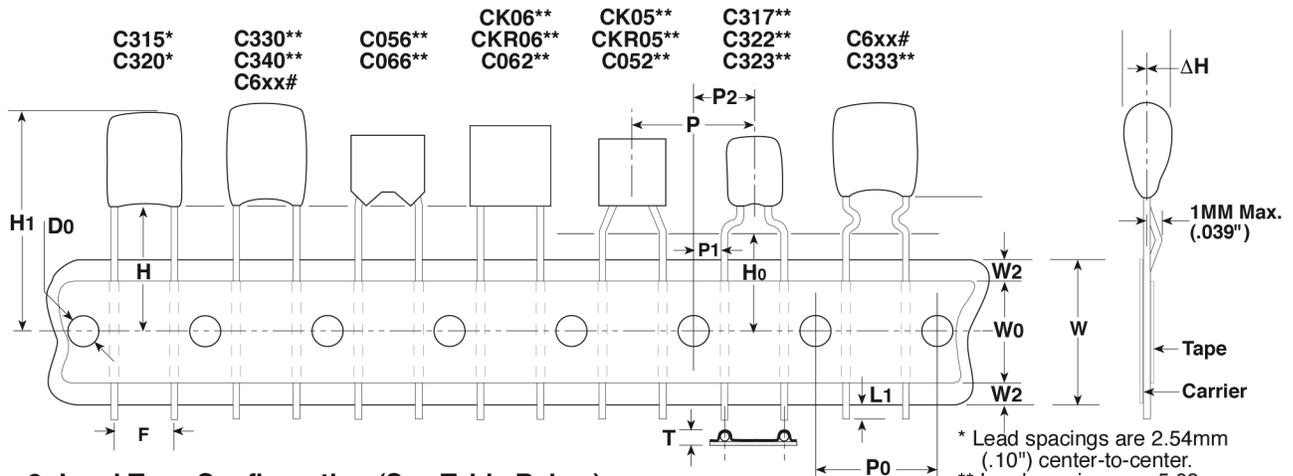


Figure 2: Lead Tape Configuration (See Table Below)

* Lead spacings are 2.54mm (.10") center-to-center.
 ** Lead spacings are 5.08mm (.20") center-to-center.
 # See page 22 for exact lead configuration for Series.

Ceramic Radial Tape and Reel Dimensions in Millimeters (Inches)

Dimension	Symbol	Nominal mm (inch)	Tolerance mm (inch)	Dimension	Symbol	Nominal mm (inch)	Tolerance mm (inch)
Sprocket Hole Diameter	D0	4.0 (.157)	± 0.2 (.008)	Height to Seating Plane (formed leads) (2)	H0	7301 7303 16.0 (.630) 18.0 (.709)	7301 7303 ±0.5 (.020) Minimum
Sprocket Hole Pitch	P0	12.7 (.500)	± 0.3 (.012)	Component Alignment	Δh	4.0 (.157)	±0.2 (.008)
Component Pitch	P	12.7 (.500)	± 0.3 (.012)	Lead Protrusion	L1	1.0 (.039)	Maximum
Lead Spacing (1)	F	5.08 (.20) 2.54 (.10)	+0.6 -0.2 (+.024 -.008)	Composite Tape Thickness	t	0.7 (.051)	±0.2 (.008)
Sprocket Hole Center to Lead Center (1)	P1	3.81 (.150) 5.08 (.200)	± 0.7 (.028)	Overall Tape and Lead Thickness	T	1.5 (.059)	Maximum
Sprocket Hole Center to Component Center	P2	6.35 (.250)	± 1.3 (.051)	Carrier Tape Width	W	18.0 (.709)	+1.0 -0.5 (+.039 -.020)
Height to Seating Plane (straight leads) (2)	H	7301 7303 16.0 (.630) 18.0 (.709)	7301 7303 ±0.5 (.020) Minimum	Hold-Down Tape Width	W0	5.0 (.197)	Minimum
Component Height Above Tape Center	H1	32.2 (1.27)	Maximum	Hold-Down Tape Location	W2	3.0 (.118)	Maximum

(1) Measured at the egress from the carrier tape, on the component side.
 (2) Determined by a 4 digit suffix placed at the end of the part number, as follows:
 7301 = Recommended for parts with formed leads. Example: C322C104K5R5CA7301
 7303 = Recommended for parts with straight leads. Example: C320C104K5R5CA7303

CERAMIC PACKAGING						
KEMET Series	Military Style	Military Specification	Standard (1) Bulk Quantity	Ammo Pack Quantity Maximum	Maximum Reel Quantity	Reel Size
C114C-K-G	CK12, CC75	MIL-C-11015/	200/Box		5000	12"
C124C-K-G	CK13, CC76	MIL-PRF-20	200/Box		5000	12"
C192C-K-G	CK14, CC77		100/Box		3000	12"
C202C-K	CK15		25/Box		500	12"
C222C-K	CK16		10/Tray		300	12"
C052C-K-G	CK05, CC05		100/Bag	2000	2000	12"
C062C-K-G	CK06, CC06		100/Bag	1500	1500	12"
C114G	CCR75	MIL-PRF-20	200/Box		5000	12"
C124G	CCR76		200/Box		5000	12"
C192G	CCR77		100/Box		3000	12"
C202G	CC78-CCR78		25/Box		500	12"
C222G	CC79-CCR79		10/Tray		300	12"
C052/56G	CCR05		100/Bag		1700	12"
C062/66G	CCR06		100/Bag		1500	12"
C512G	CC07-CCR07		Footnote (2)		N/A	N/A
C522G	CC08-CCR08		Footnote (2)		N/A	N/A
C114T	CKR11	MIL-PRF-39014	200/Box		5000	12"
C124T	CKR12		200/Box		5000	12"
C192T	CKR14		100/Box		3000	12"
C202T	CKR15		25/Box		500	12"
C222T	CKR16		10/Tray		300	12"
C052/56T	CKR05		100/Bag		1700	12"
C062/66T	CKR06		100/Bag		1500	12"
C31X			500/Bag	2500	2500	12"
C32X			500/Bag	2500	2500	12"
C33X			250/Bag	1500	1500	12"
C340			100/Bag	1000	1000	12"
C350			50/Bag	N/A	500	12"
C410			300/Box	4000	5000	12"
C412			200/Box	4000	5000	12"
C420			300/Box	4000	5000	12"
C430			200/Box	2000	2500	12"
C440			200/Box	2000	2500	12"
C512	N/A	N/A	Footnote (2)		N/A	N/A
C522	N/A	N/A	Footnote (2)		N/A	N/A
C617			250/Bag		1000	12"
C622/C623			100/Bag		500	12"
C627/C628			100/Bag		500	12"
C630/C631			100/Bag		500	12"
C637/C638			50/Bag		500	12"
C640/C641			50/Bag		500	12"
C642/C643			50/Bag		500	12"
C647/C648			50/Bag		500	12"
C657/C658			50/Bag		500	12"
C667/C668			50/Bag		500	12"

NOTE: (1) Standard packaging refers to number of pieces per bag, tray or vial.

(2) Quantity varies. For further details, please consult the factory.