

BOARD ROUTING RECOMMENDATIONS

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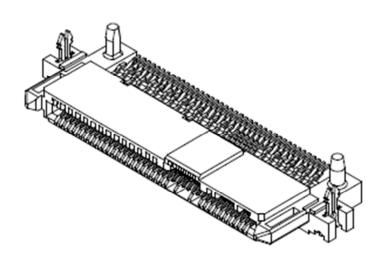


BOARD ROUTING RECOMMENDATIONS

1.0 SCOPE

This specification covers the high-speed PCB routing recommendations of high-speed signals at primary and secondary ports for 78809 series connector. The connector is a right angle surface mount type. The pins of the connector are soldered for mechanical retention to the PC board.

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2.0 PC BOARD REQUIREMENTS

2.1 MATERIAL THICKNESS

The recommended PC board thickness shall be 3.00mm. Suitable PC board material shall be glass epoxy (FR-4).

2.2 LAYOUT

The solder pads for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Refer to the applicable Sales Drawing for the recommended solder pad pattern, dimensions and tolerances.

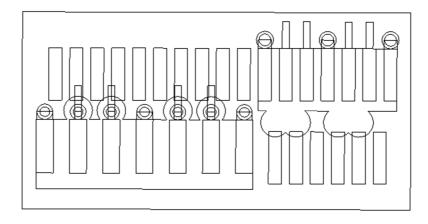
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BOARD ROUTING RECOMMENDATIONS

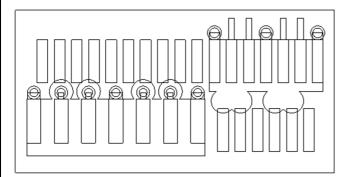
3.0 HIGH-SPEED ROUTING

3.1 GENERAL ROUTING EXAMPLE (other configurations are possible)

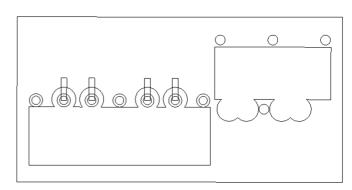


Only high-speed signals at primary and secondary ports are shown. Showing connector footprint, 2 high-speed signal layers and 1 reference ground layer overlaid. Routing example shown for reference only.

1st signal layer with reference layer



2nd signal layer with reference layer



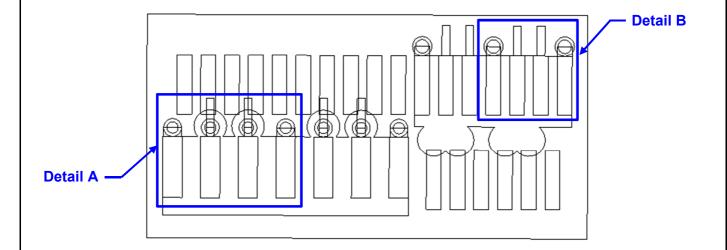
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BOARD ROUTING RECOMMENDATIONS

3.2 HIGH-SPEED TRANSMISSION LINE PLANE



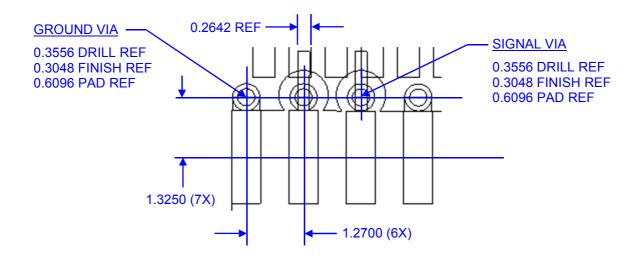
Only high-speed signals at primary and secondary ports are shown. Shown with connector footprint and 1 reference ground layer. Routing example shown for reference only.

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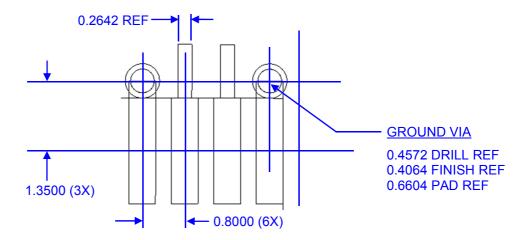


BOARD ROUTING RECOMMENDATIONS

Detail A (Applicable to SAS Primary Port)



Detail B (Applicable to both SAS Secondary and PCIe Ports)



Note: Trace width and via dimensions above can vary from recommendation to meet board thickness, routing and electrical requirements.

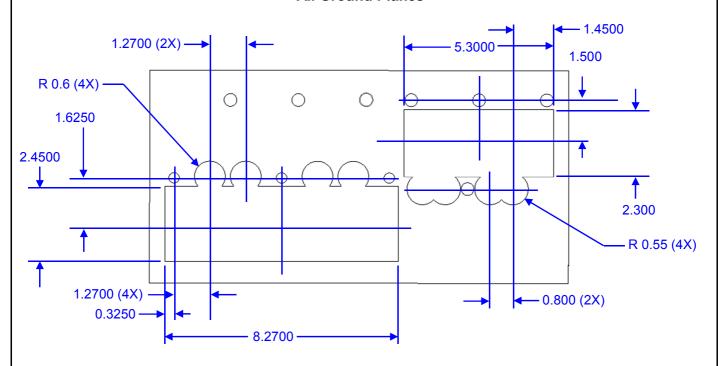
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BOARD ROUTING RECOMMENDATIONS

3.3 HIGH-SPEED REFERENCE PLANE ANTI-PAD





Note: Anti-pad was implemented for impedance matching. Dimensions can vary from recommendation to meet electrical requirements. The anti-pad can be made larger with a broader keep-out region on non-signal ground planes to minimize parasitic capacitance.

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BOARD ROUTING RECOMMENDATIONS

3.4 TRACE TO PAD ATTACHMENT & GROUND VIA PLACEMENT (FOR BOTH MICROSTRIP AND STRIPLINE ROUTING)

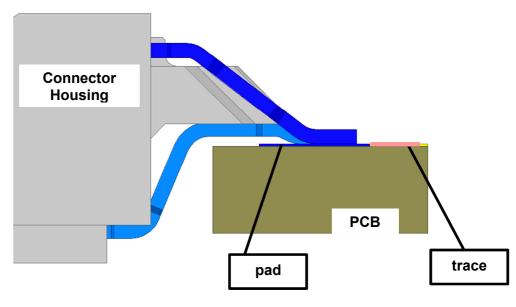


Figure 1

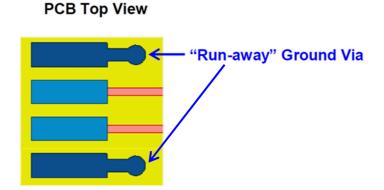


Figure 2

As seen in Figure 1, with connector at edge of board, the trace will be routed outwards from pad of connector. Due to routing constrain, "run-away" ground vias from ground pads should follow the direction where the signal traces were attached to their corresponding signals pads as shown in Figure 2.

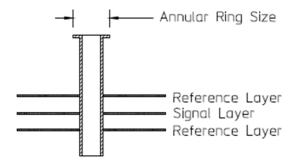
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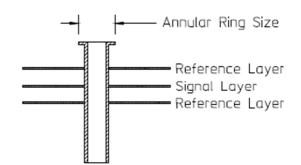
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BOARD ROUTING RECOMMENDATIONS

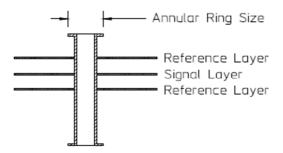
3.5 SIGNAL THROUGH-HOLE VIA STUBS (FOR STRIPLINE ROUTING)

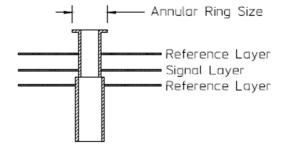




Bottom Launch
Driven Via
(Preferred)

Top Launch
Stub Via
(Worst Case)





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Standard Via Configuration

Back Drill To Minimize Stub

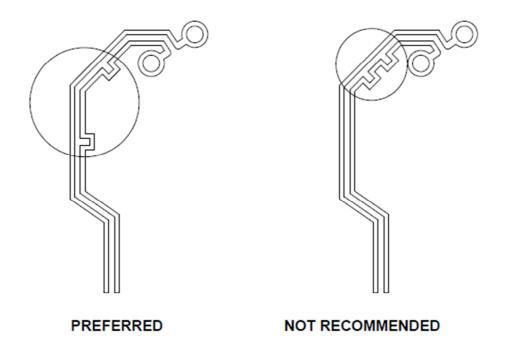
Only the signal reference ground planes are shown above and only two annular rings are required for retention of the through-hole via within the printed circuit board. Non-functional annular rings should be removed for unassociated signal layers.

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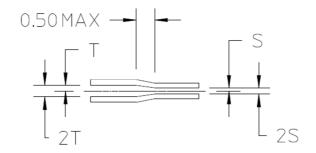
BOARD ROUTING RECOMMENDATIONS

3.6 SKEW COMPENSATION FOR DIFFERENTIAL ROUTING



It is recommended that skew compensation be distributed verses grouped in one or more locations.

3.7 TRACE COMPARISON



TRANSITION SHOULD BE SYMMETRIC

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