CM1230

2, 4, and 8-Channel Low-Capacitance ESD Protection Array

ON Semiconductor®

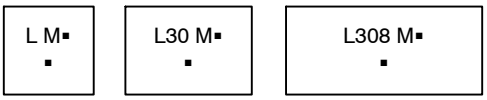
http://onsemi.com

WLCSP4
CP SUFFIX
CASE 567CS

WLCSP6
CP SUFFIX
CASE 567BB

WLCSP10
CP SUFFIX
CASE 567BG

MARKING DIAGRAM



CSP−4 CSP−6 CSP−10

Lxxx = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
CM1230−02CP (Note 1)	CSP−4 (Pb−Free)	3,500/Tape & Reel
CM1230−J2CP (Note 1)	CSP−4 (Pb−Free)	3,500/Tape & Reel
CM1230−04CP	CSP−6 (Pb−Free)	3,500/Tape & Reel
CM1230−08CP	CSP−10 (Pb−Free)	3,500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*Standard test condition is IEC61000−4−2 level 4 test circuit with each (A_{OUT}/B_{OUT}) pin subjected to ±12 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run.

1. CM1230−02CP and CM1230−J2CP are the same mechanical package. Only difference is the Pin 1 orientation ('+' mark) on the tape and reel.

Product Description

The CM1230 is a family of 2, 4 and 8 channel, very low capacitance ESD protection diode arrays in a CSP form factor. It is ideal for protecting systems with high data and clock rates or for circuits that need low capacitive loading. Each channel consists of a pair of ESD diodes that act as clamp diodes to steer ESD current pulses to either the positive or negative supply rail. A Zener diode is integrated between the positive and negative supply rails. The V_{CC} rail is protected from ESD strikes and eliminates the need for a bypass capacitor to absorb positive ESD strikes to ground. Each channel can safely dissipate ESD strikes of ±8 kV, meeting the Level 4 requirement of the IEC61000−4−2 international standard as well as ±15 kV air discharges per the IEC61000−4−2 specification. Using the MIL−STD−883 (Method 3015) specification for Human Body Model (HBM) ESD, the pins are protected for contact discharges at greater than ±15 kV.

This device is well−suited for next generation wireless handsets that implement high−speed serial interface solutions for the LCD display and camera interfaces. In these designs, a tolerance above 1.5 pF cannot be tolerated when high data rates are transferred between the baseband choppiest and the LCD driver/controller Is. Higher capacitive loading normally causes the rise and fall times to slow which hampers the functionality of circuit and operation of the wireless handset. The CM1230 incorporates *OptiGuard*™ which results in improved reliability at assembly. The CM1230 is available in a space−saving, low profile Chip Scale Package with RoHS−compliant, lead−free finishing.

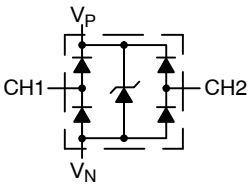
Features

- Two, Four, and Eight Channels of ESD Protection
- Provides ESD Protection to IEC61000−4−2 Level 4 ±8 kV Contact Discharge & ±15 kV Air Discharge
- Low Loading Capacitance of 0.8 pF Typical
- Minimal Capacitance Change with Temperature and Voltage
- Channel I/O to GND Capacitance Difference of 0.02 pF Typical is Ideal for Differential Signals
- Channel I/O to I/O Capacitance 0.15 pF Typical
- Zener Diode Protects Supply Rail and Eliminates the Need for External By−pass Capacitors
- Each I/O Pin Can Withstand Over 1000 ESD Strikes*
- Available in 4, 6 and 10 Bump Chip Scale Packages (CSP)
- *OptiGuard*™ Coated for Improved Reliability at Assembly
- These Devices are Pb−Free and are RoHS Compliant

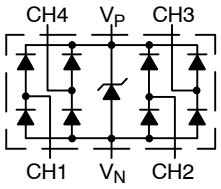
Applications

- I/O Port Protection for Mobile Handsets, Notebook Computers, DSCs, MP3 Players, PDAs, etc. Including USB, 1394 and Serial ATA
- LCD and Camera Data Lines in Wireless Handsets that use High−speed Serial Interfaces
- Wireless Handsets
- Handheld PCs/PDAs
- LCD and Camera Modules

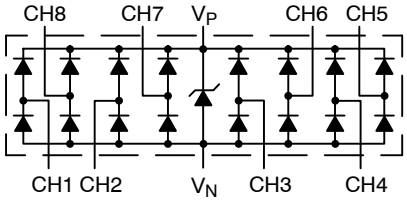
ELECTRICAL SCHEMATIC



CM1230−02CP/
CM1230−J2CP



CM1230−04CP



CM1230−08CP

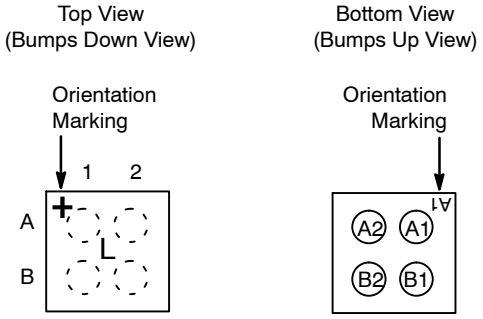
Table 1. PIN DESCRIPTIONS

2−Channel, 4−Bump CSP			
Pin	**Name**	**Type**	**Description**
A1	V_N	GND	Negative Voltage Supply Rail
B1	CH2	I/O	ESD Channel
A2	CH1	I/O	ESD Channel
B2	V_P	PWR	Positive Voltage Supply Rail

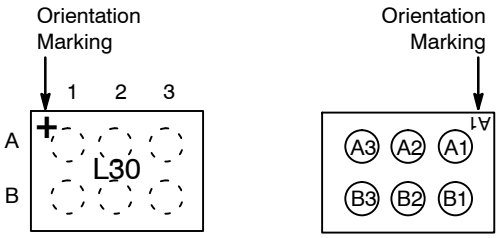
4−Channel, 6−Bump CSP			
Pin	**Name**	**Type**	**Description**
A1	CH1	I/O	ESD Channel
B1	CH2	I/O	ESD Channel
A2	V_P	PWR	Positive Voltage Supply Rail
B2	V_N	GND	Negative Voltage Supply Rail
A3	CH3	I/O	ESD Channel
B3	CH4	I/O	ESD Channel

8−Channel, 10−Bump CSP			
Pin	**Name**	**Type**	**Description**
A1	CH1	I/O	ESD Channel
B1	CH2	I/O	ESD Channel
A2	CH3	I/O	ESD Channel
B2	CH4	I/O	ESD Channel
A3	V_P	PWR	Positive Voltage Supply Rail
B3	V_N	GND	Negative Voltage Supply Rail
A4	CH5	I/O	ESD Channel
B4	CH6	I/O	ESD Channel
A5	CH7	I/O	ESD Channel
B5	CH8	I/O	ESD Channel

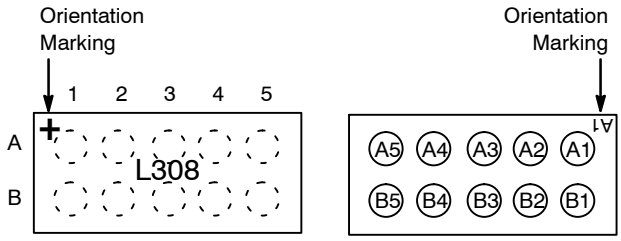
PACKAGE / PINOUT DIAGRAMS



CM1230−02/J2
4−bump CSP Package



CM1230−04
6−bump CSP Package



CM1230−08
10−bump CSP Package

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Supply Voltage (V_P – V_N)	6.0	V
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–65 to +150	°C
DC Voltage at any Channel Input	(V_N – 0.5) to (V_P + 0.5)	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	–40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_P	Operating Supply Voltage (V_P–V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P–V_N) = 3.3 V			8.0	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8 mA; T_A = 25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	V
I_{LEAK}	Channel Leakage Current	T_A = 25°C; V_P = 5 V, V_N = 0 V, V_{IN} = 0 V to 5 V		±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P = 3.3 V, V_N = 0 V, V_{IN} = 1.65 V		0.80	1.2	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, V_P = 3.3 V, V_N = 0 V, V_{IN} = 1.65 V		0.02		pF
C_{MUTUAL}	Mutual Capacitance between signal pin and adjacent signal pin	At 1 MHz, V_P = 3.3 V, V_N = 0 V, V_{IN} = 1.65 V		0.15		pF
V_{ESD}	In–system ESD Protection Peak Discharge Voltage at any channel input, in system a) Contact discharge per IEC 61000–4–2 standard b) Human Body Model, MIL–STD–883, Method 3015	 T_A = 25°C (Notes 4 and 5) T_A = 25°C (Notes 3 and 5)	 ±8 ±15			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1A, t_P = 8/20 μS (Note 5)		 +9.8 –1.8		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1 A, t_P = 8/20 μS Any I/O pin to Ground (Note 5)		 0.76 0.56		Ω

2. All parameters specified at T_A = –40°C to +85°C unless otherwise noted.
3. Human Body Model per MIL–STD–883, Method 3015, $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 KΩ, V_P = 3.3 V, V_N grounded.
4. Standard IEC 61000–4–2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω, V_P = 3.3 V, V_N grounded.
5. These measurements performed with no external capacitor on V_P.
6. Measured under pulsed conditions, pulse width = 0.7 ms, maximum current = 1.5 A.

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

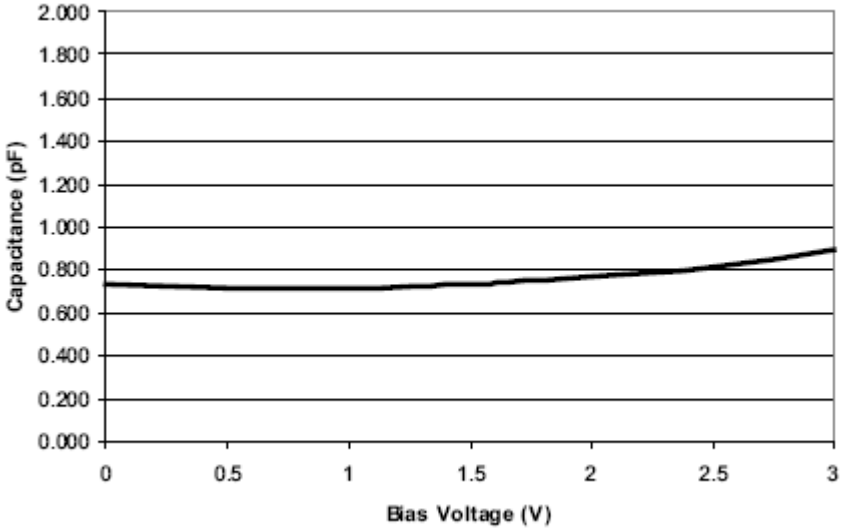


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
(f = 1 MHz, V_P = 3.3 V, V_N = 0 V, 0.1 μF chip capacitor between V_P and V_N, T_A = 25°C)

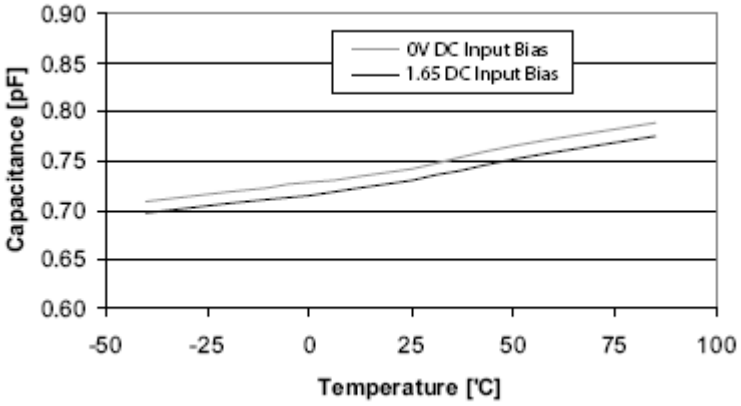


Figure 2. Typical Variation of C_{IN} vs. Temp
(f = 1 MHz, V_{IN} = 30 mV, V_P = 3.3 V, V_N = 0 V, 0.1 μF chip capacitor between V_P and V_N)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ω Environment)

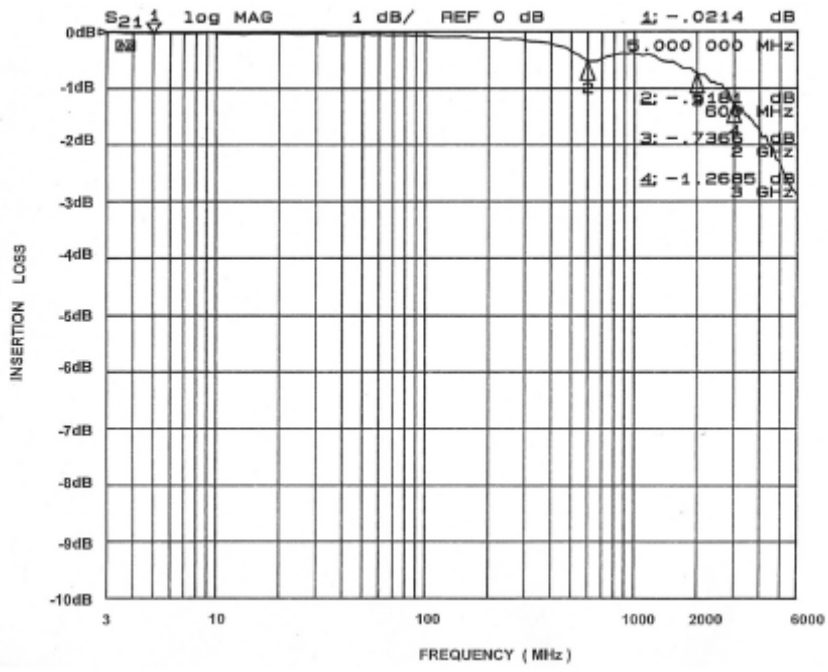


Figure 3. Insertion Loss vs. Frequency (0 V DC Bias, V_P = 3.3 V)

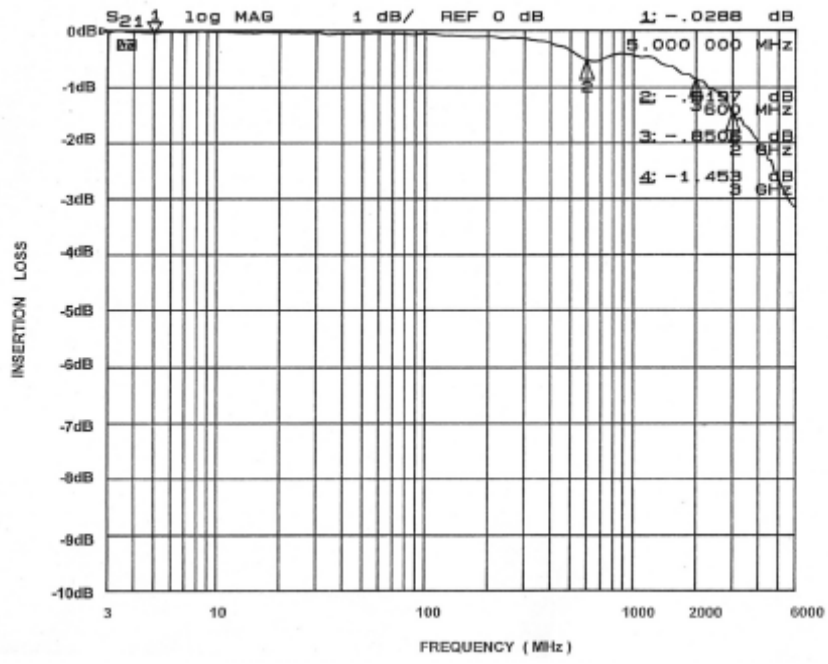


Figure 4. Insertion Loss vs. Frequency (2.5 V DC Bias, V_P = 3.3 V)

APPLICATION INFORMATION

Table 5. PRINTED CIRCUIT BOARD RECOMMENDATIONS

Parameter	Value
Pad Size on PCB	0.275 mm
Pad Shape	Round
Pad Definition	Non−Solder Mask defined pads
Solder Mask Opening	0.325 mm Round
Solder Stencil Thickness	0.125 − 0.150 mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.330 mm Round
Solder Flux Ratio	50/50 by volume
Solder Paste Type	No Clean
Pad Protective Finish	OSP (Entek Cu Plus 106A)
Tolerance − Edge To Corner Ball	±50 μm
Solder Ball Side Coplanarity	±20 μm
Maximum Dwell Time Above Liquidous	60 seconds
Maximum Soldering Temperature for Lead−free Devices using a Lead−free Solder Paste	260°C

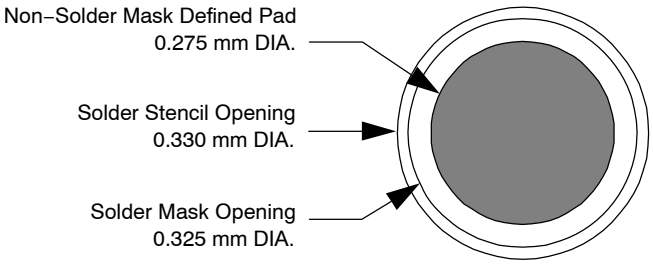


Figure 5. Recommended Non−Solder Mask Defined Pad Illustration

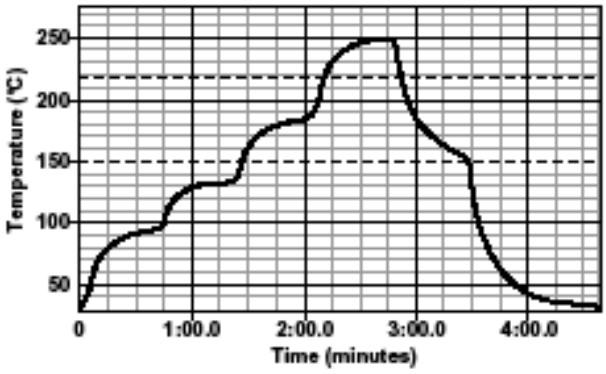
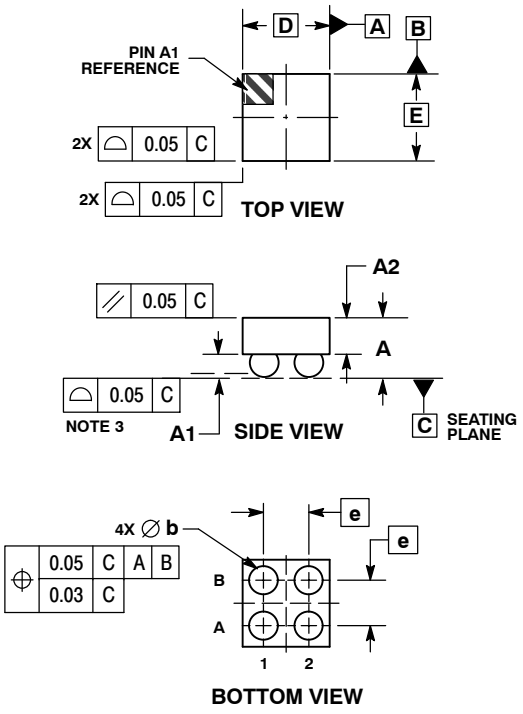


Figure 6. Lead−free (SnAgCu) Solder Ball Reflow Profile

PACKAGE DIMENSIONS

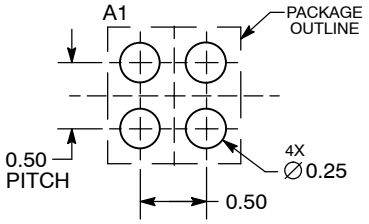
WLCSP4, 0.96x0.96
CASE 567CS
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.61	0.69
A1	0.21	0.28
A2	0.41 REF	
b	0.29	0.34
D	0.96 BSC	
E	0.96 BSC	
e	0.50 BSC	

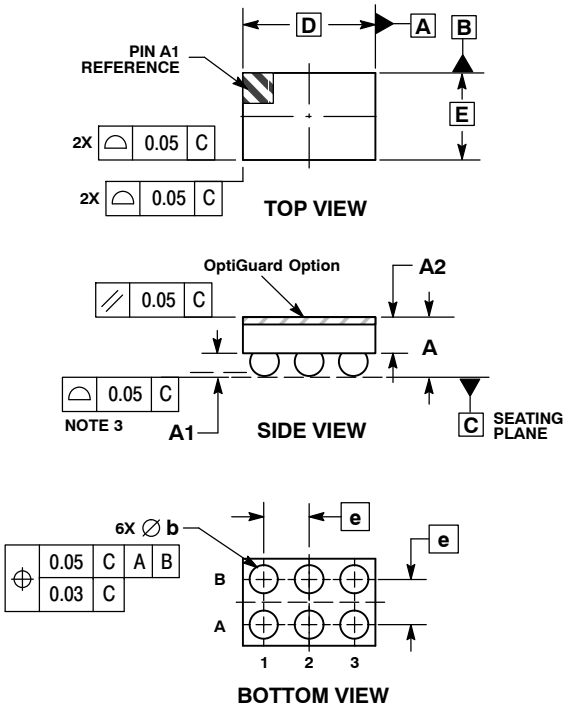
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

WLCSP6, 1.46x0.96
CASE 567BB
ISSUE O



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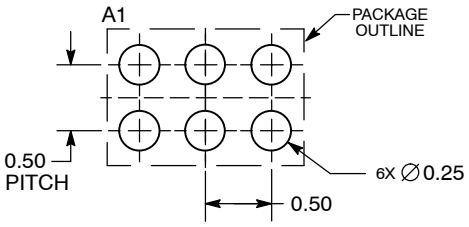
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.56	0.72
A1	0.21	0.27
A2	0.42 REF	
b	0.29	0.35
D	1.46 BSC	
E	0.96 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

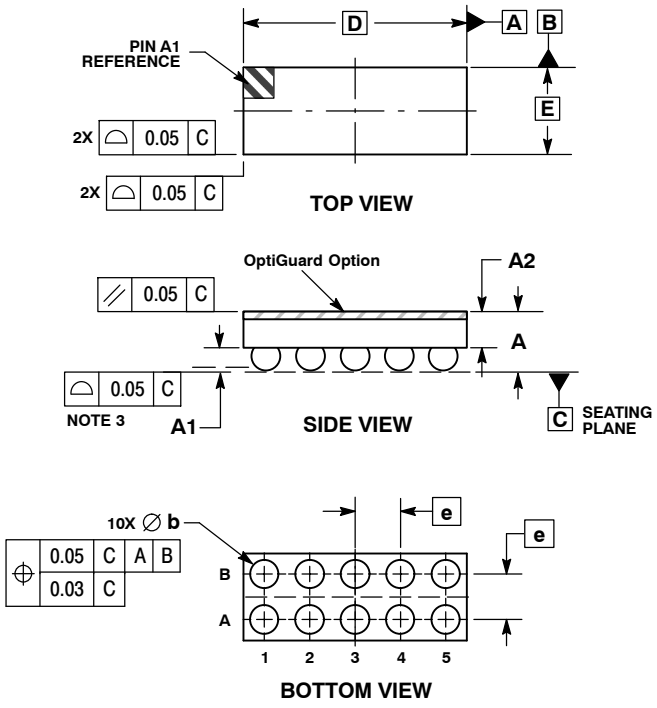


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WLCSP10, 2.46x0.96
CASE 567BG
ISSUE O



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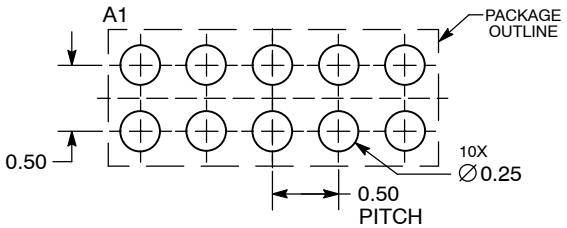
A2	0.42 REF	
b	0.29	0.35
D	2.46 BSC	
E	0.96 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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PUBLICATION ORDERING INFORMATION

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