

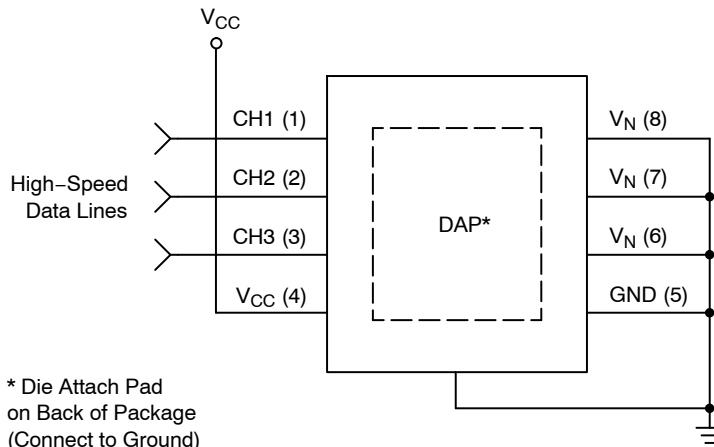
# CM1641

## 4-Channel Low Capacitance Dual-Voltage ESD Protection Array

### Features

- Three Channels of Low Voltage ESD Protection
- One Channel of High Voltage ESD Protection
- Provides ESD Protection to IEC61000-4-2 Level 4:
  - ◆  $\pm 8$  kV Contact Discharge (Pins 1-3)
  - ◆  $\pm 15$  kV Contact Discharge (Pin 4)
- Low Channel Input Capacitance
- Minimal Capacitance Change with Temperature and Voltage
- High Voltage Zener Diode Protects Supply Rail
- No Need for External Bypass Capacitors
- Each I/O Pin can Withstand over 1000 ESD Strikes\*
- These Devices are Pb-Free and are RoHS Compliant

### TYPICAL APPLICATION



Note: All grounds must be connected.



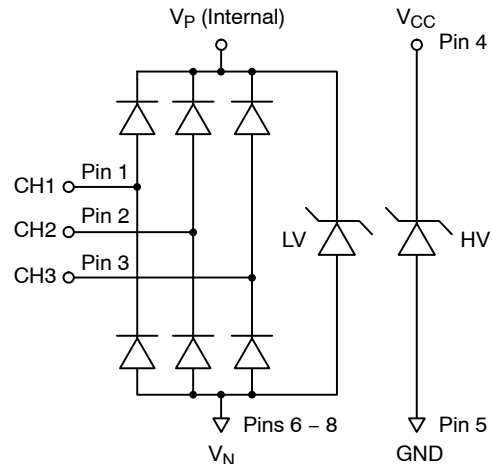
ON Semiconductor®

<http://onsemi.com>



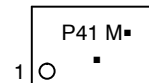
UDFN8  
D4 SUFFIX  
CASE 517BC

### ELECTRICAL SCHEMATIC



Note: Pins 5 and 6 to 8 are connected to a common substrate.

### MARKING DIAGRAM



P41 = CM1641-04D4  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
CM1641-04D4	UDFN-8 0.4 mm (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

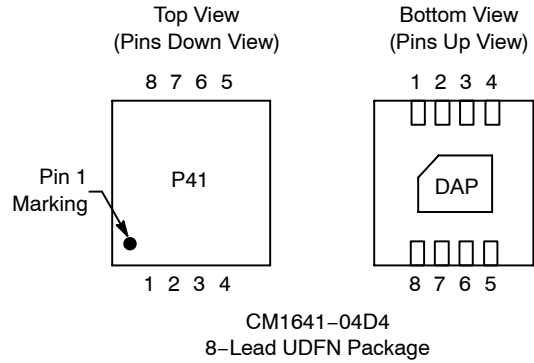
\*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to  $\pm 8$  kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

# CM1641

**Table 1. PIN DESCRIPTIONS**

4-Channel, 8-Lead, UDFN-8 Package			
Pin	Name	Type	Description
1	CH1	I/O	LV Low-capacitance ESD Channel
2	CH2	I/O	LV Low-capacitance ESD Channel
3	CH3	I/O	LV Low-capacitance ESD Channel
4	V <sub>CC</sub>	HV V <sub>DD</sub>	HV ESD Channel
5	GND	-	Ground
6	V <sub>N</sub>	-	Negative Voltage Supply Rail
7	V <sub>N</sub>	-	Negative Voltage Supply Rail
8	V <sub>N</sub>	-	Negative Voltage Supply Rail
DAP	GND	-	Die Attach Pad (Ground)

**PACKAGE / PINOUT DIAGRAMS**



## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Rating	Units
DC Voltage on Low-Voltage Pins	6.0	V
DC Voltage on High-Voltage Pins (V <sub>CC</sub> pin)	14.5	V
Storage Temperature Range	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. STANDARD OPERATING CONDITIONS**

Parameter	Rating	Units
Operating Temperature Range	-40 to +85	°C

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>F</sub>	LV Diode Reverse Voltage (Positive Voltage)	I <sub>F</sub> = 10 mA, T <sub>A</sub> = 25°C	6.8	8.2	9.2	V
	LV Diode Forward Voltage (Negative Voltage)	I <sub>F</sub> = 10 mA, T <sub>A</sub> = 25°C	-1.05	-0.90	-0.60	
I <sub>LEAK</sub>	LV Channel Leakage Current	T <sub>A</sub> = -30°C to 65°C, V <sub>IN</sub> = 3.3 V V <sub>N</sub> = 0 V			100	nA
C <sub>IN</sub>	LV Channel Input Capacitance	At 1 MHz, V <sub>N</sub> = 0 V, V <sub>IN</sub> = 1.65 V		1.2	1.5	pF
ΔC <sub>IN</sub>	LV Channel Input Capacitance Matching	At 1 MHz, V <sub>N</sub> = 0 V, V <sub>IN</sub> = 1.65 V		0.02		pF
I <sub>LEAK_HV</sub>	HV Channel Leakage Current	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 11 V, V <sub>N</sub> = 0 V		0.1	1.0	μA
C <sub>IN_HV</sub>	HV Channel Input Capacitance	At 1 MHz, V <sub>N</sub> = 0 V, V <sub>IN</sub> = 2.5 V		53		pF
V <sub>F_HV</sub>	HV Diode Breakdown Voltage Positive Voltage	I <sub>F</sub> = 10 mA, T <sub>A</sub> = 25°C	14.6		17.7	V
V <sub>ESD</sub>	ESD Protection Peak Discharge Voltage at any channel input, in system Contact Discharge per IEC 61000-4-2 Standard	T <sub>A</sub> = 25°C	±8 (Pin 1-3) ±15 (Pin 4)			kV

# CM1641

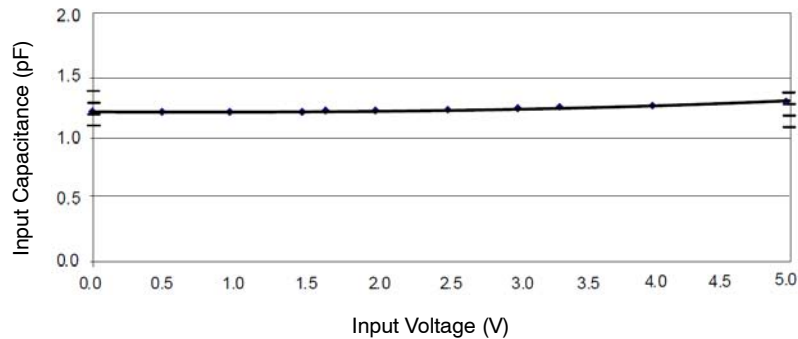
**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{CL}$	LV Channel Clamp Voltage (Pin 1-3) Positive Transients Negative Transients	$T_A = 25^\circ\text{C}$ , $I_{PP} = 1\text{ A}$ , $t_P = 8/20\ \mu\text{S}$		+9.64 -1.75		V
$R_{DYN}$	Dynamic Resistance LV Channel Positive Transients LV Channel Negative Transients HV Channel Positive Transients HV Channel Negative Transients	$I_{PP} = 1\text{ A}$ , $t_P = 8/20\ \mu\text{S}$ Any I/O Pin to Ground		0.72 0.59 1.20 0.36		$\Omega$

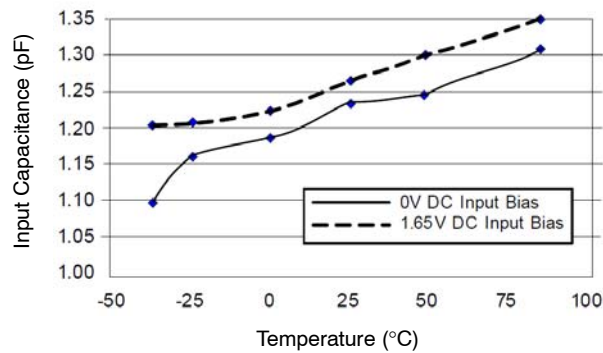
1. All parameters specified at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.

## PERFORMANCE INFORMATION

### Input Channel Capacitance Performance Curves for Low Voltage Pins



**Figure 1. Typical Variation of  $C_{IN}$  vs.  $V_{IN}$**   
(Low Voltage Inputs,  $f = 1\text{ MHz}$ ,  $V_N = 0\text{ V}$ )



**Figure 2. Typical Variation of  $C_{IN}$  vs. Temperature**  
(Low Voltage Inputs,  $f = 1\text{ MHz}$ ,  $V_N = 0\text{ V}$ )

# CM1641

## PERFORMANCE INFORMATION (Cont'd)

### Typical Filter Performance for Low Voltage Pins

Nominal conditions unless specified otherwise, 50  $\Omega$  Environment.

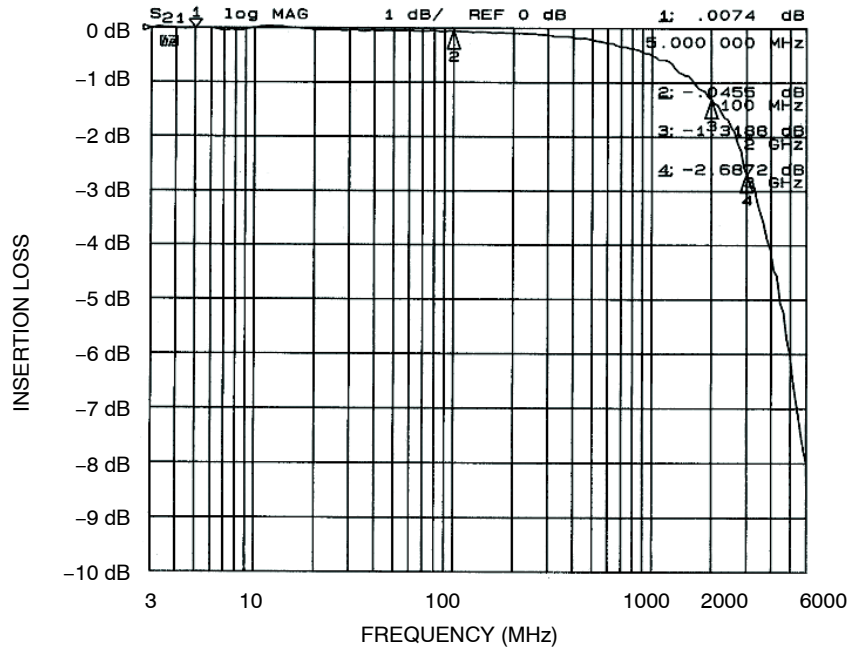


Figure 3. Channel 1 vs. All GND Pins (0 V DC Bias)

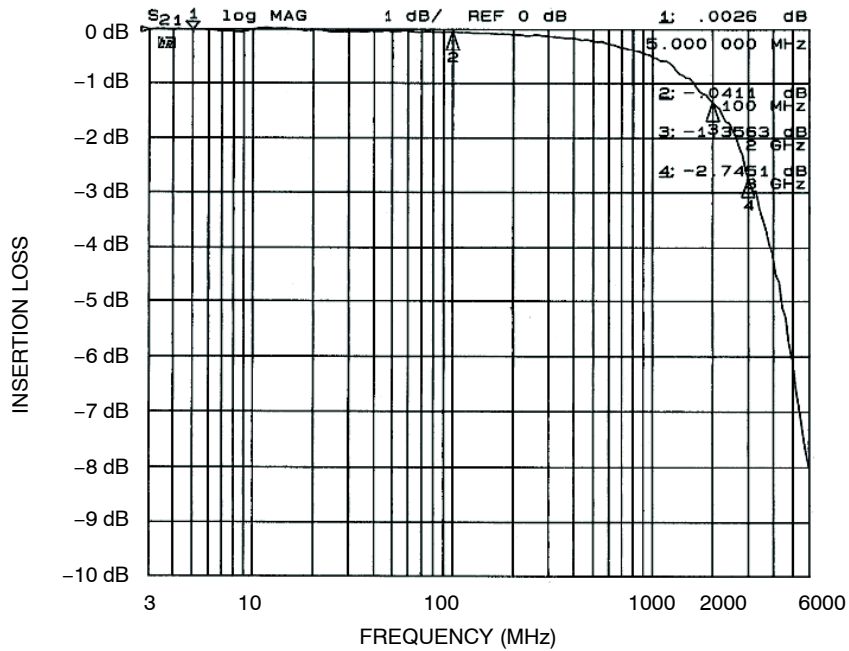


Figure 4. Channel 2 vs. All GND Pins (0 V DC Bias)

# CM1641

## PERFORMANCE INFORMATION (Cont'd)

### Typical Filter Performance for Low Voltage Pins

Nominal conditions unless specified otherwise, 50  $\Omega$  Environment.

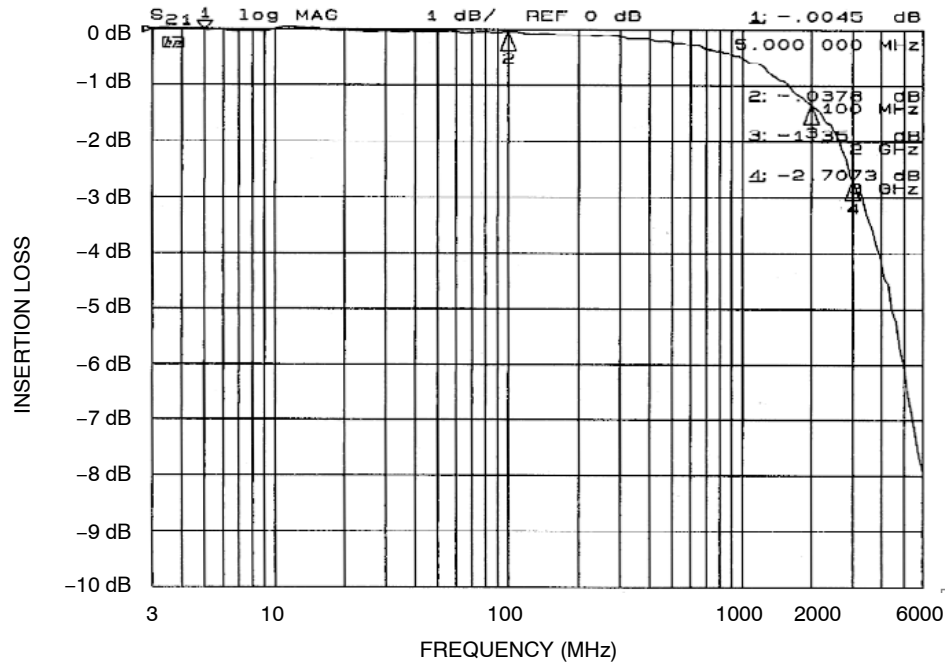
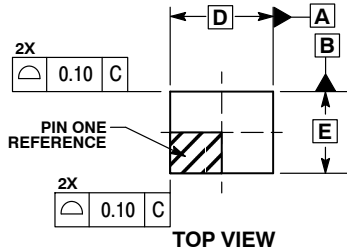


Figure 5. Channel 3 vs. All GND Pins (0 V DC Bias)

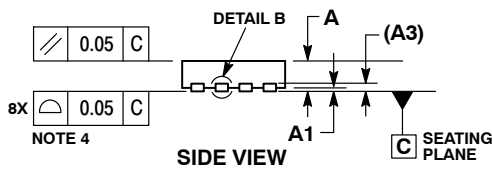
# CM1641

## PACKAGE DIMENSIONS

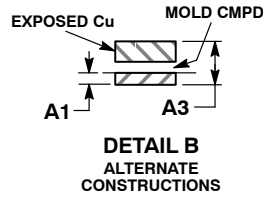
UDFN8, 1.7x1.35, 0.4P  
CASE 517BC-01  
ISSUE 0



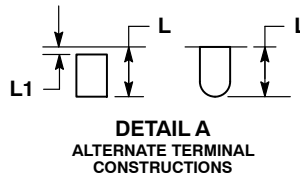
TOP VIEW



SIDE VIEW



DETAIL B  
ALTERNATE  
CONSTRUCTIONS

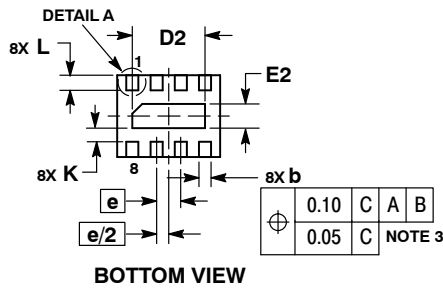


DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS

NOTES:

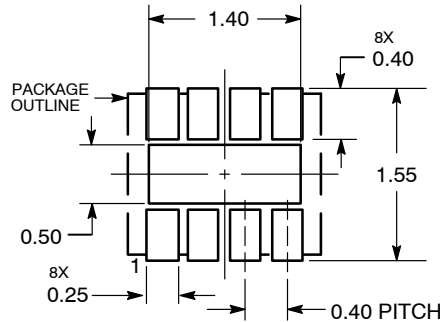
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.70	BSC
D2	1.10	1.30
E	1.35	BSC
E2	0.30	0.50
e	0.40	BSC
K	0.15	---
L	0.20	0.30
L1	---	0.05



BOTTOM VIEW

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5773-3850

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)  
Order Literature: <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative