ESD8040

Transient Voltage Suppressors

Low Capacitance ESD Protection for High Speed Video Interface

The ESD8040 transient voltage suppressor is designed specifically to protect HDMI and Display Port with full functionality ESD protection and back drive current protection for V_{CC} line. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance for the high speed TMDS lines.

Features

- Full Function HDMI / Display Port Solution
- Single Connect, Flow through Routing for TMDS Lines
- Low Capacitance (0.35 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 Level 4
- UL Flammability Rating of 94 V−0
- This is a Pb−Free Device

Typical Applications

- HDMI
- Display Port

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.

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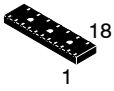
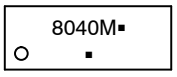
MARKING DIAGRAM



UDFN18
CASE 517CP



8040 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
ESD8040MUTAG	UDFN18 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

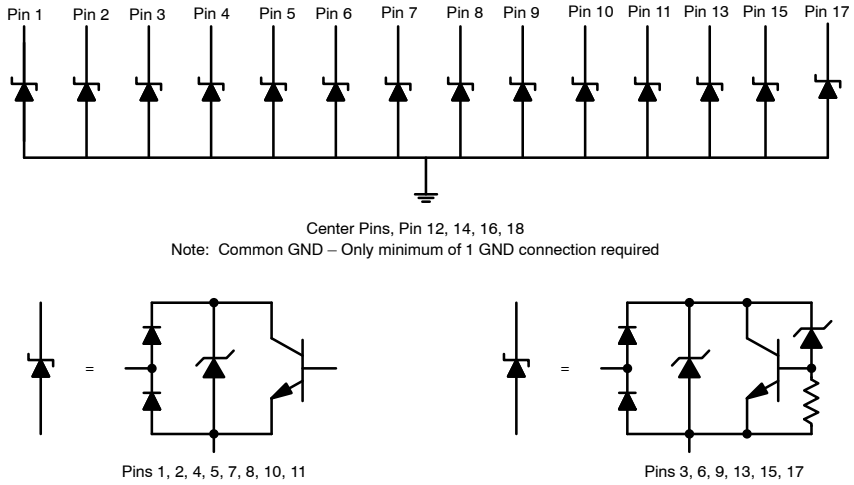


Figure 1. Pin Schematic

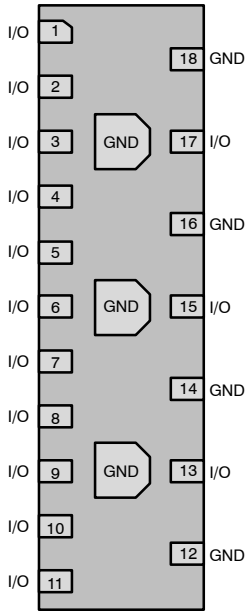


Figure 2. Pin Configuration

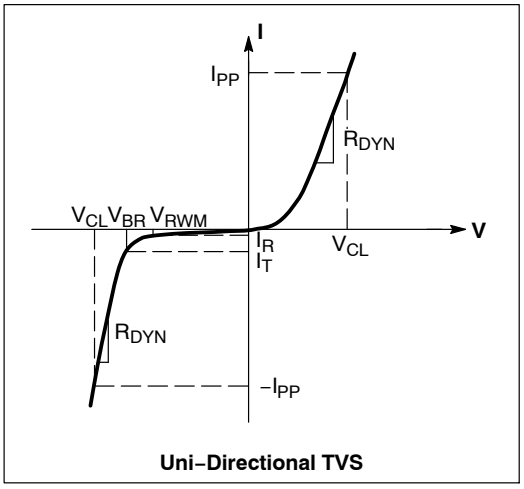
Note: Pins 12, 14, 16, 18 and center pins are connected internally as a common ground.
Only minimum of one pin needs to be connected to ground for functionality of all pins.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
R_{DYN}	Dynamic Resistance

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pins 1, 2, 4, 5, 7, 8, 10, 11 to GND I_T = 1 mA, I/O Pins 3, 6, 9, 13, 15, 17 to GND	4.0 5.5	5.5 6.5		V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND			1.0	μA
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 kV Contact	See Figures 3 and 4			V
Clamping Voltage TLP (Note 2) See Figures 7 through 10	V_C	I_{PP} = 8 A I_{PP} = −8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air) I_{PP} = 16 A I_{PP} = −16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)		9.3 −4.8 12.9 −8.9		V
Dynamic Resistance	R_{DYN}	I/O Pin to GND GND to I/O Pin		0.44 0.50		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.30	0.35	pF

1. For test procedure see Figures 5 and 6 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

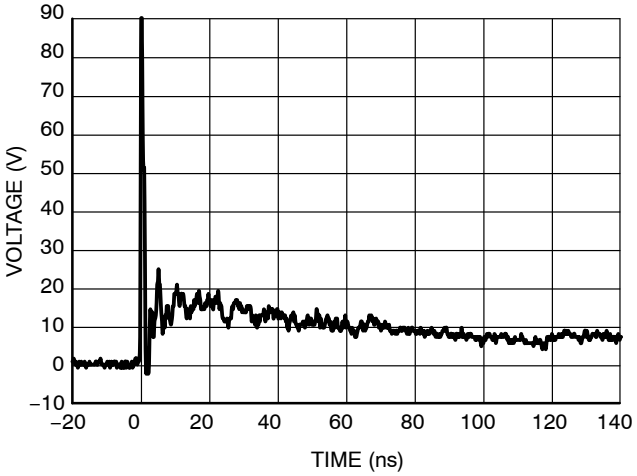


Figure 3. IEC61000−4−2 +8 kV Contact Clamping Voltage

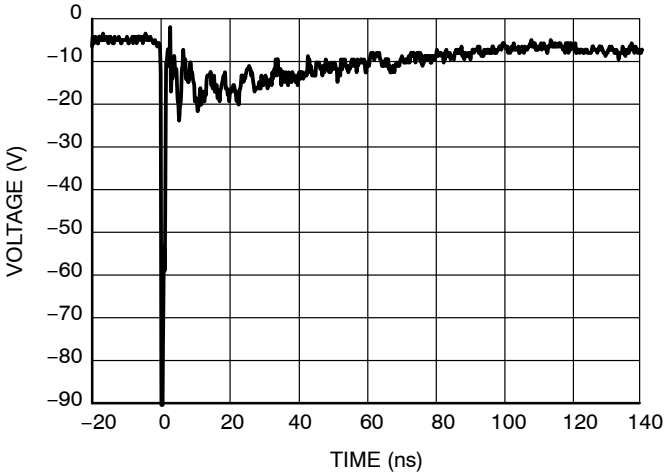


Figure 4. IEC61000−4−2 −8 kV Contact Clamping Voltage

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

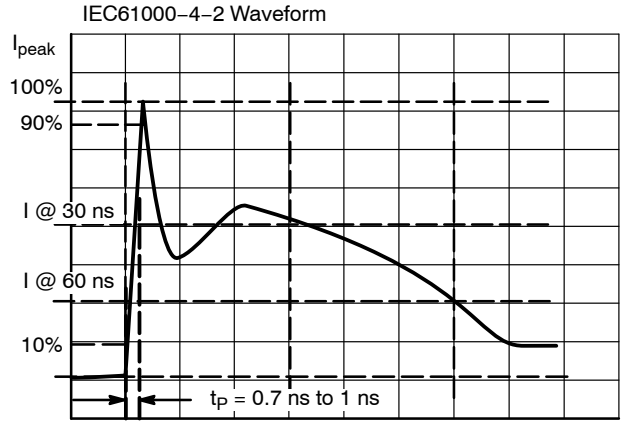


Figure 5. IEC61000−4−2 Spec

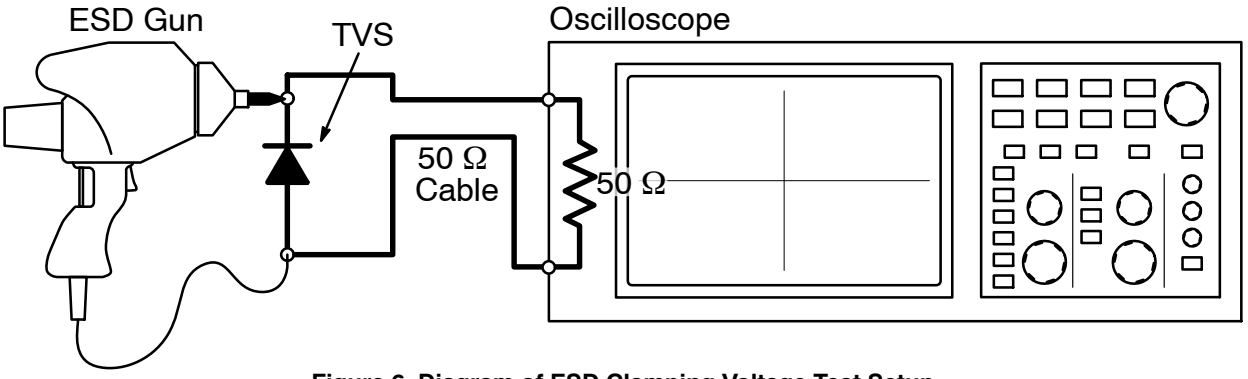


Figure 6. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

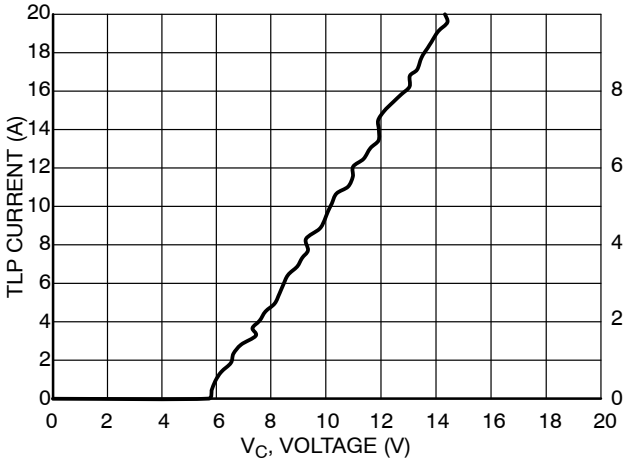


Figure 7. Positive TLP I−V Curve

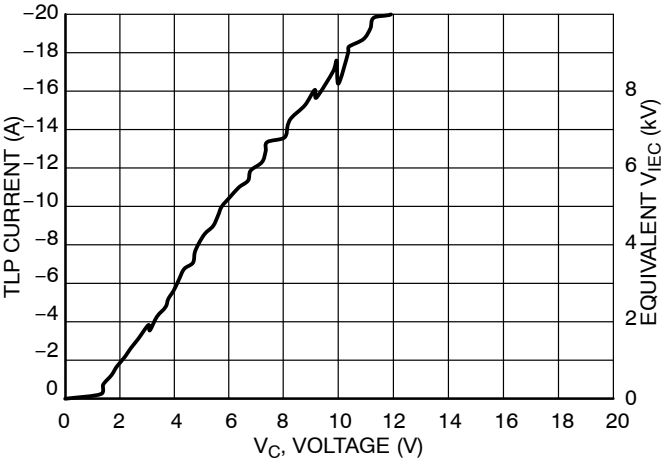


Figure 8. Negative TLP I−V Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

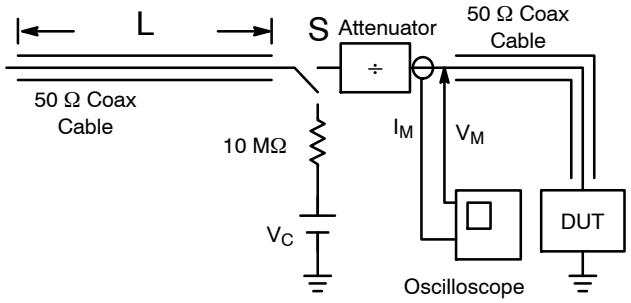


Figure 9. Simplified Schematic of a Typical TLP System

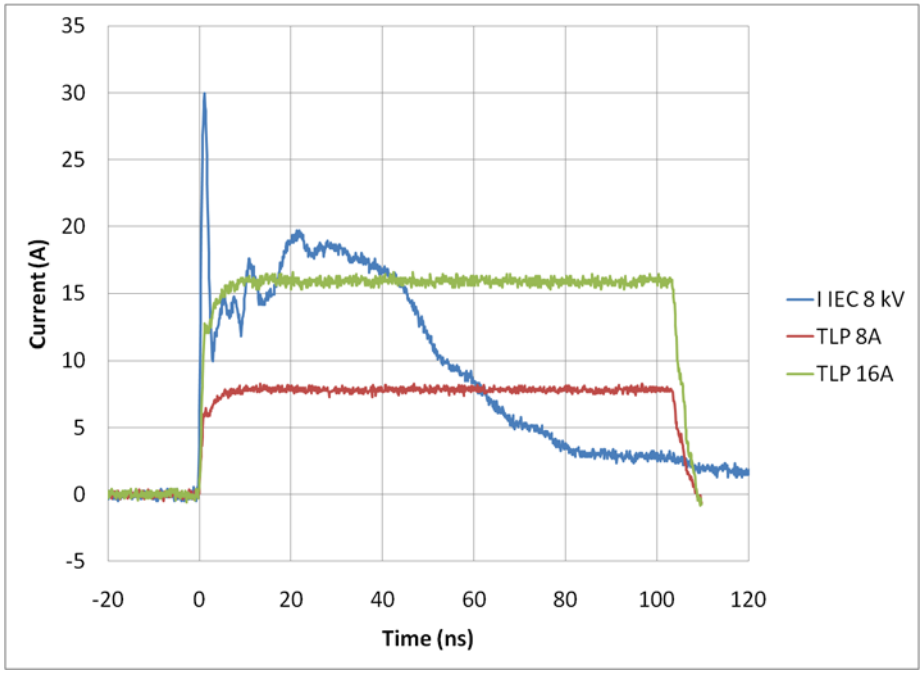


Figure 10. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

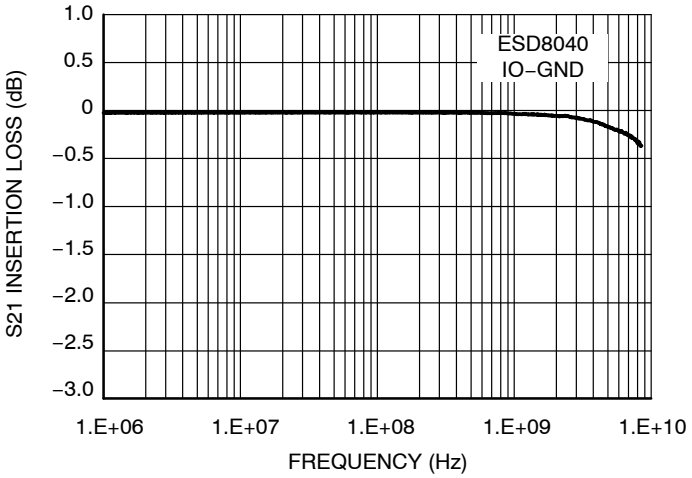


Figure 11. ESD8040 Insertion Loss

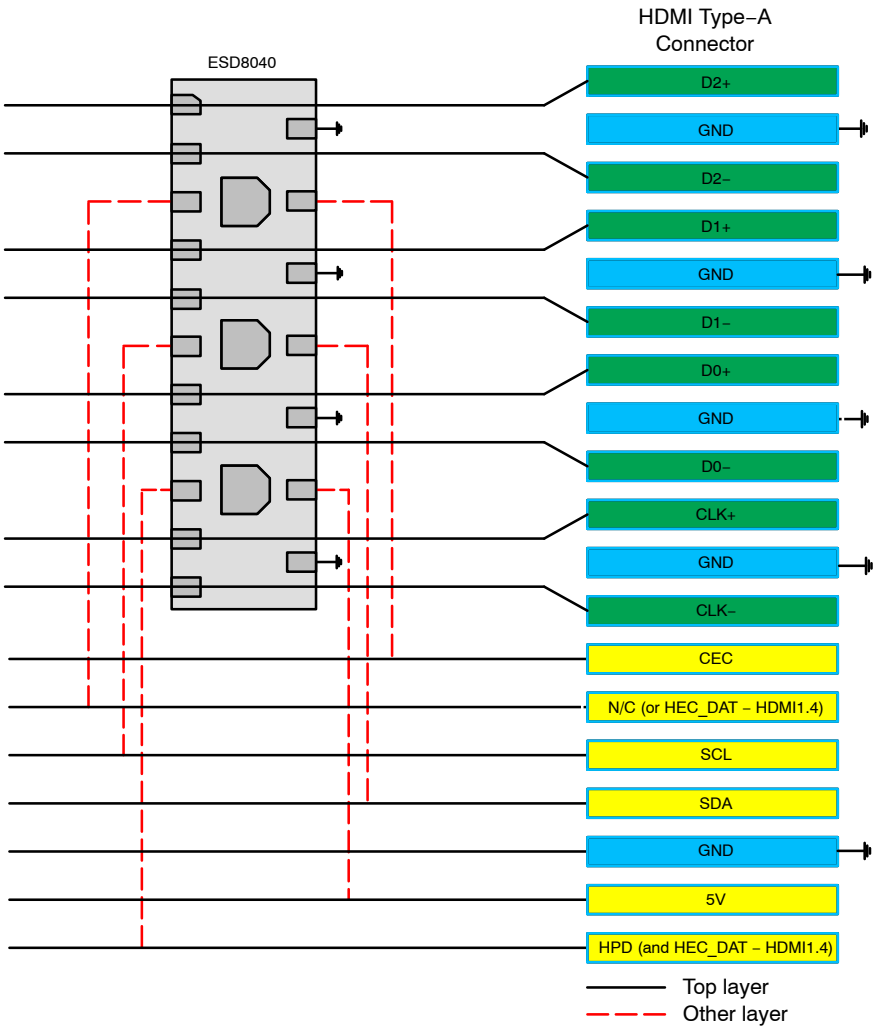
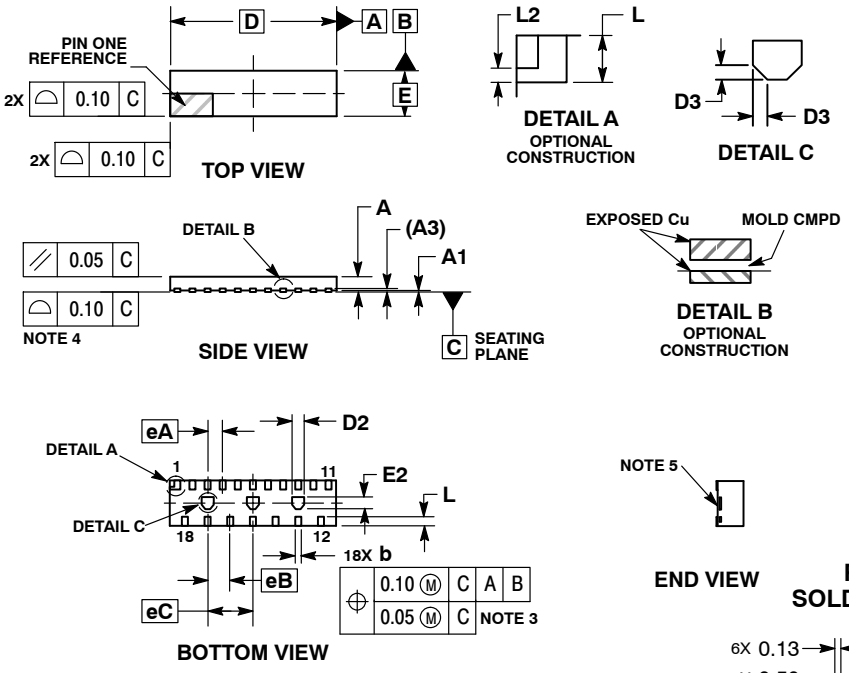


Figure 12. HDMI Layout Diagram

IO pins 1, 2, 4, 5, 7, 8, 10, and 11 are to be used for high speed differential TMDS lines whereas IO pins 3, 6, 9, 13, 15, and 17 are to be used for lower speed lines (I^2C, CEC, HPD, etc.). The ESD8040 was designed specifically for the HDMI application. The IO pins for TMDS lines have a lower breakdown voltage and faster turn−on in the low current region in order to better protect the sensitive low voltage, high−speed TMDS signals. The IO pins for lower speed lines have a higher breakdown voltage to accommodate the higher voltages associated with the HPD, CEC, I^2C and V_{CC} lines as well as the optional Ethernet pin that can be implemented in HDMI1.4a applications.

PACKAGE DIMENSIONS

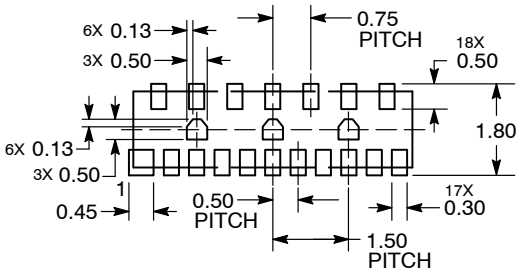
UDFN18, 5.5x1.5, 0.5P/0.75P
CASE 517CP
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED ENDS OF TERMINALS ARE ELECTRICALLY ACTIVE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	5.50 BSC	
D2	0.35	0.45
D3	0.10 REF	
E	1.50 BSC	
E2	0.35	0.45
eA	0.50 BSC	
eB	0.75 BSC	
eC	1.50 BSC	
L	0.20	0.40
L2	0.10 REF	

RECOMMENDED SOLDERING FOOTPRINT*



NOTE: CENTER PADS OPTIONAL DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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