SPECIFICATION FOR

TDK MULTILAYER CERAMIC CHIP CAPACITORS

CUSTOMER	DWG.NO.
Digi Key Corporation	C2004-579
TDK ITEM	DATE ISSUED
Mega Cap Series	Mar. 24, 2004

TDK ENGINEERING SIGNATURE

DRAWN BY	CHECKED BY	APPROVED BY
Etsuko Mifune		
DATE Mar. 24 2004	DATE Mar. 26, 2004	DATE Mar. 26 2004

Please return this specification to TDK representatives.
If orders are placed without returned specification, please allow us to judge that specification is accepted by your side.

CUSTOMER RESPONSE

☐ Accept

☐ Accept with the following changes

☐ Reject with the following reasons

CUSTOMER SIGNATURE	TITLE	DATE

TDK CORPORATION
13-1,Nihonbashi 1-chome,Chuo-ku,Tokyo 103-8272,Japan
Phone : Tokyo(03)3278-5111

1. SCOPE

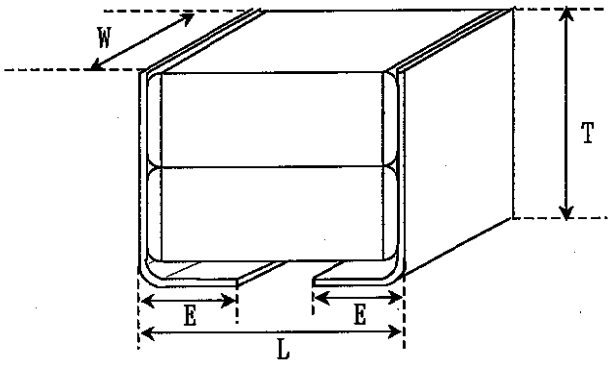
This specification is applicable to chip type multilayer ceramic capacitors with a priority over the other relevant specifications.
Production places defined in this specification shall be TDK Corporation Japan, TDK Taiwan Corporation, TDK Xiamen Co.,Ltd, TDK Dalian Corporation, TDK(Suzhou)Co.,Ltd, Korea TDK Co.,Ltd, TDK(Malaysia)Sdn.Bhd, TDK Components U.S.A. Inc, TDK(Thailand) Co.,Ltd and TDK Hungary Ltd.

EXPLANATORY NOTE:
This specification warrants the quality of the ceramic chip capacitor. The chips should be evaluated or confirmed a state of mounted on your product.
If the use of the chips go beyond the bounds of the specification, we can not afford to guarantee.

2. CODE CONSTRUCTION

(Example)	CKG57N	X7R	2 E	105	M	T
	(1)	(2)	(3)	(4)	(5)	(6)

(1)Type



Type	Dimensions (Unit : mm)			
TDK(EIA style)	L	W	T	E
CKG45N	5.5 max.	4.0 max.	5.5 max.	1.4 max.
CKG57N	6.5 max.	5.5 max.	5.5 max.	1.9 max.

(2)Temperature Characteristics (Details are shown in para.8 No.7)

(3)Rated Voltage

Symbol	Rated Voltage
2 J	DC 630 V
2 E	DC 250 V
2 A	DC 100 V
1 H	DC 50 V
1 E	DC 25 V
1 C	DC 16 V

(4)Rated Capacitance

Stated in three digits and in units of pico farads (pF). The first and Second digits identify the first and second significant figures of the Capacitance, the third digit identifies the multiplier.

Example 105 → 1,000,000pF

(5)Capacitance tolerance

Symbol	Tolerance
M	±20 %

(6)Packaging

Symbol	Packaging
T	Taping

3. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
X7R	-55°C	125°C	25°C
X5R	-55°C	85°C	25°C

4. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH

6 months Max.

5.RECOMMENDATION

It is recommended to provide a slit (about 1mm) on the board under the components to improve washing Flux. And please make sure to dry detergent up completely before using.

6.RECOMMENDED CONDITION FOR SOLDERING

Soldering is limited to Reflow soldering.

Metal cap is jointed by high temp solder, however the solder temperature must be less than 250°C to avoid melting the solder.

See page-15 for the soldering.

7. INDUSTRIAL WASTE DISPOSAL

Dispose this product as industrial waste in accordance with the Industrial Waste Law.

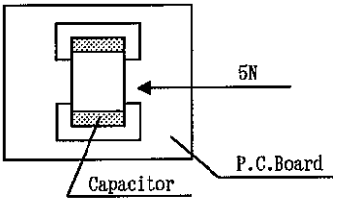
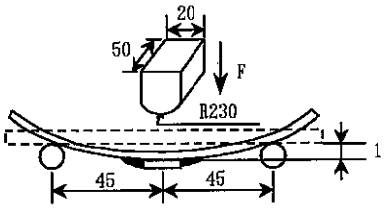
8. PERFORMANCE

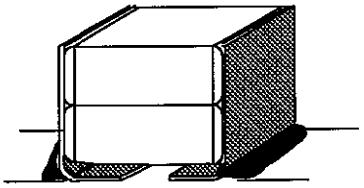
table 1

<table>
<tr><th>No.</th><th>Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>1</td><td>External Appearance</td><td>No defects which may affect performance.</td><td>Inspect with magnifying glass(3×)</td></tr>
<tr><td>2</td><td>Insulation Resistance</td><td>500 MΩ・μF min.(As for the capacitor of rated voltage 16V DC, 100 MΩ・μF min.)</td><td>Apply rated voltage for 60s.
As for the capacitor of rated voltage 630V DC, apply 500V DC.</td></tr>
<tr><td>3</td><td>Voltage Proof</td><td>Withstand test voltage without insulation breakdown or other damage.</td><td><table><tr><th>Rated voltage</th><th>Withstand voltage</th></tr><tr><td>16V, 25V
50V, 100V</td><td>2.5 times of rated voltage</td></tr><tr><td>250V, 630V</td><td>1.5 times of rated voltage</td></tr></table>Above DC voltage shall be applied for 1～5s.
Charge / discharge current shall not exceed 50mA.</td></tr>
<tr><td>4</td><td>Capacitance</td><td>Within the specified tolerance.</td><td><table><tr><th>Rated Capacitance</th><th>Measuring frequency</th><th>Measuring voltage</th></tr><tr><td>10μF and under</td><td>1kHz±10%</td><td>1.0±0.2V rms.</td></tr><tr><td>Over 10μF</td><td>120Hz±20%</td><td>0.5±0.2V rms.</td></tr></table></td></tr>
<tr><td>5</td><td>Dissipation Factor</td><td><table><tr><th>T.C.</th><th>Rated Voltage</th><th>D.F.</th></tr><tr><td rowspan="2">X7R</td><td>16V DC</td><td>0.05 max.</td></tr><tr><td>25V DC and over</td><td>0.03 max.</td></tr><tr><td rowspan="2">X5R</td><td>16V DC</td><td>0.075 max.</td></tr><tr><td>25V DC and over</td><td>0.05 max.</td></tr></table></td><td><table><tr><th>Rated Capacitance</th><th>Measuring frequency</th><th>Measuring voltage</th></tr><tr><td>10μF and under</td><td>1kHz±10%</td><td>1.0±0.2V rms.</td></tr><tr><td>Over 10μF</td><td>120Hz±20%</td><td>0.5±0.2V rms.</td></tr></table></td></tr>
<tr><td>6</td><td>Ripple current</td><td>Heat generation
ΔT : 20℃ max.</td><td>Reflow solder the capacitor on a P.C.Board shown in Appendix 2 and apply voltage with 10kHz～1MHz sine curve.
(Ripple voltage Vp-p to be under rated voltage.)</td></tr>
<tr><td>7</td><td>Temperature Characteristics of Capacitance</td><td><table><tr><th>Capacitance Change(%)</th></tr><tr><td>No voltage applied</td></tr><tr><td>X5R : ±15
X7R : ±15</td></tr></table></td><td>Capacitance shall be measured by the steps shown in the following table, after thermal equilibrium is obtained for each step.
ΔC be calculated ref. STEP3 reading.<table><tr><th>Step</th><th>Temperature(℃)</th></tr><tr><td>1</td><td>Reference temp. per para.3. ±2</td></tr><tr><td>2</td><td>Min. operating temp. per para.3. ±2</td></tr><tr><td>3</td><td>Reference temp. per para.3. ±2</td></tr><tr><td>4</td><td>Max. operating temp. per para.3. ±2</td></tr></table></td></tr>
</table>

TDK

(continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>8</td><td colspan="2">Robustness of Terminations</td><td>No sign of termination coming off, breakage of ceramic, or other abnormal signs.</td><td>Reflow solder the capacitor on a P.C.Board shown in Appendix2 and apply a pushing force of 5N for 10±1s.
 
</td></tr>
<tr><td>9</td><td colspan="2">Bending</td><td>No mechanical damage.</td><td>Reflow solder the capacitor on a P.C.Board shown in Appendix1 and Bend it for 1mm.
 

(Unit : mm)</td></tr>
<tr><td>10</td><td colspan="2">Solderability</td><td>Both end faces and the contact areas shall be covered with a smooth and bright solder coating with no more than a small amount of scattered imperfections such as pinholes or un-wetted or de-wetted areas.
These imperfections shall not be concentrated in one area.
  </td><td>Reflow solder the capacitor on a P.C.Board shown in Appendix 2.

Solder : H63A(JIS Z 3282)

Flux : Isopropyl alcohol(JIS K 8839)
Rosin(JIS K 5902)
25% solid solution.</td></tr>
<tr><td rowspan="5">11</td><td rowspan="5">Temperature cycle</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow Solder the capacitors on a P.C.Board shown in Appendix2 before testing.

Expose the capacitors in the condition step1 through 4 and repeat 100 times consecutively.

Leave the capacitors in ambient condition for 48±4h before measurement.

<table><tr><th>Step</th><th>Temperature (℃)</th><th>Time (min.)</th></tr><tr><td>1</td><td>Min. operating temp. per para 3. ±3</td><td>30±3</td></tr><tr><td>2</td><td>Reference Temp.</td><td>2～5</td></tr><tr><td>3</td><td>Max. operating temp. per para 3. ±2</td><td>30±2</td></tr><tr><td>4</td><td>Reference Temp.</td><td>2～5</td></tr></table></td></tr>
<tr><td>Capacitance</td><td><table><tr><th>Characteristics</th><th>Change from the value before test</th></tr><tr><td>X5R
X7R</td><td>±7.5 %
±7.5 %</td></tr></table></td></tr>
<tr><td>D.F.</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>Voltage proof</td><td>No insulation breakdown or other damage.</td></tr>
</table>

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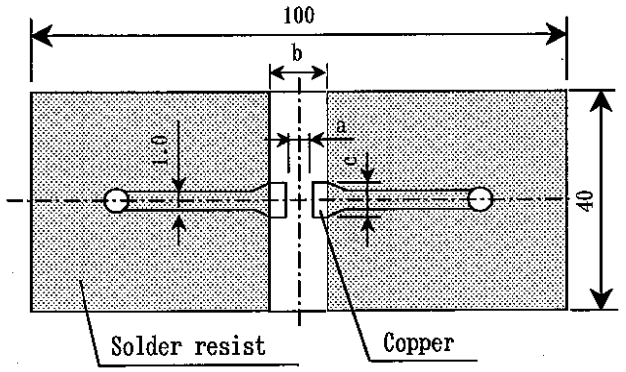
(continued)

No.	Item		Performance	Test or inspection method
12	Moisture Resistance	External appearance	No mechanical damage.	Reflow Solder the capacitors on a P.C.Board shown in Appendix2 before testing. Apply the rated voltage at temperature 40±2°C and 90 to 95%RH for 500 +24,0h. Charge/discharge current shall not exceed 50mA. Leave the capacitors in ambient condition for 48±4h before measurement. Voltage conditioning Voltage treat the capacitor under testing temperature and voltage for 1hour. Leave the capacitors in ambient condition for48±4h before measurement. Use this measurement for initial value.
		Capacitance	Characteristics: X5R, X7R Change from the value before test: ±12.5 %, ±12.5 %	
		D.F.	characteristics X5R : 200% of initial spec max. X7R : 200% of initial spec max.	
		Insulation Resistance	25 MΩ · μF min.(As for the capacitor of rated voltage 16V DC, 5 MΩ · μF min.)	
13	Life	External appearance	No mechanical damage.	Reflow Solder the capacitors on a P.C.Board shown in Appendix2 before testing. X7R : Apply 2× rated voltage at 125±2°C for 1,000 +48,0h. (DC250V:×1.5, DC630V:×1.2) X5R : Apply 2× rated voltage at 85±2°C for 1,000 +48,0h. Charge/discharge current shall not exceed 50mA. Leave the capacitors in ambient condition for 48±4h before measurement. Voltage conditioning Voltage treat the capacitor under testing temperature and voltage for 1hour. Leave the capacitors in ambient condition for48±4h before measurement. Use this measurement for initial value.
		Capacitance	Characteristics: X5R, X7R Change from the value before test: ±15 %, ±15 %	
		D.F.	characteristics X5R : 200% of initial spec max. X7R : 200% of initial spec max.	
		Insulation Resistance	50 MΩ · μF min.(As for the capacitor of rated voltage 16V DC, 10 MΩ · μF min.)	

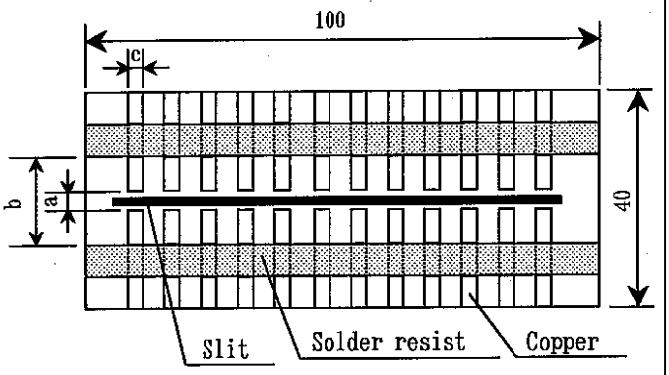
*As for the initial measurement of capacitors on number 7 and 11, leave capacitors at 150 –10,0°C for 1h and measure the value after leaving capacitors for 48±4h in ambient condition.

Appendix1

P. C. Board for bending test



Appendix2



(Unit : mm)

Type	Dimensions		
TDK(EIA style)	a	b	c
CKG45N	3.5	7.0	3.7
CKG57N	4.5	8.0	5.0

1. Material : Glass Epoxy(As per JIS C6484 GE4)

2. Thickness : 1.6mm

Copper(Thickness:0.035mm)

Solder resist

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CAPACITANCE RANGE

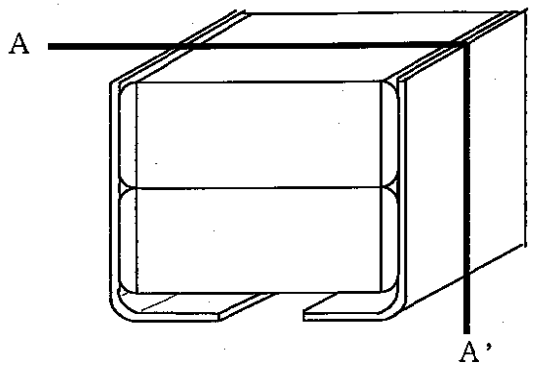
(1) CKG45N type

CAPACITANCE RANGE						
T.C.	CAPACITANCE (μF)					
	WV:DC630V	WV:DC250V	WV:DC100V	WV:DC 50V	WV:DC 25V	WV:DC 16V
X7R	0.22 (0.1μF×2)	0.47 (0.22μF×2)	1.5 (0.68μF×2)	3.3 (1.5μF×2)	10 (4.7μF×2)	22 (10μF×2)
X5R	—	—	—	10 (4.7μF×2)	—	47 (22μF×2)

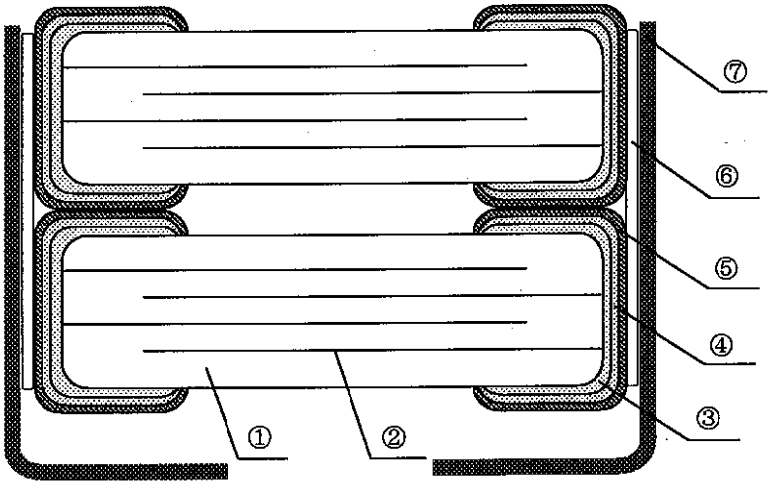
(2) CKG57N type

CAPACITANCE RANGE						
T.C.	CAPACITANCE (μF)					
	WV:DC630V	WV:DC250V	WV:DC100V	WV:DC 50V	WV:DC 25V	WV:DC 16V
X7R	0.47 (0.22μF×2)	1 (0.47μF×2)	2.2 (1μF×2) 4.7 (2.2μF×2)	6.8 (3.3μF×2)	22 (10μF×2)	33 (15μF×2)
X5R	—	—	—	22 (10μF×2)	47 (22μF×2)	100 (47μF×2)

INSIDE STRUCTURE AND MATERIAL



A－A'



No.	NAME	MATERIAL
①	Dielectric	$BaTiO_3$
②	Electrode	Ni
③	Termination	Cu
④		Ni
⑤		Sn
⑥	Metal cap joint	High temp solder
⑦	Metal cap	42 Alloy

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PACKAGING

1.SCOPE

This specification is applicable to the bulk packaging of chip type multilayer ceramic capacitors. When questionable matters are found regarding the specification products, this specification shall be applicable with priority and the matters shall be settled with written documents upon conferring and confirming between the Design Groups of both companies.

2.BULK PACKAGING

2-1 Each plastic bag shall be adhered with a label showing the following information.

1) Inspection No.
2) TDK P/N
3) Customer's P/N
4) Quantity

*Composition of Inspection No.

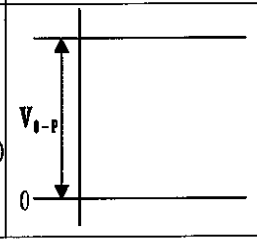
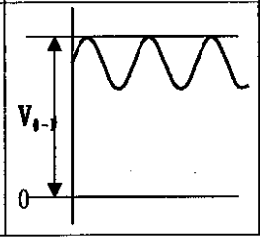
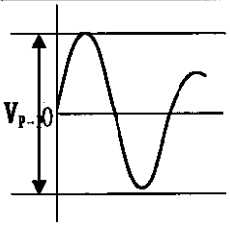
Example $\underset{(a)}{M}\ \underset{(b)}{3}\ \underset{(c)}{A} - \underset{(d)}{OO} - \underset{(e)}{OOO}$

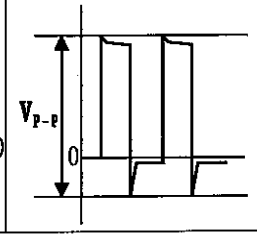
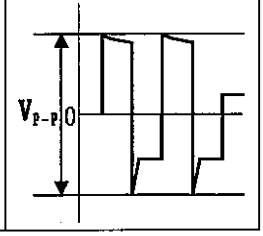
a) Line code
b) Last digit of the year
c) Month and A for January and B for February and so on.(Skip I)
d) Inspection Date of the month.
e) Serial No. of the day

2-2 Packaging and packing shall be done to protect the capacitors against damage when in transportation or storing

Caution

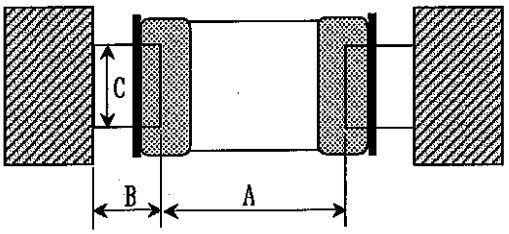
No.	Process	Condition
1	Operating Condition (Storage)	1) The capacitor must be stored in an ambient temperature of 5～40°C with a relative humidity of 20～70%RH. The products should be used within 6 months upon receipt. 2) The capacitors must be operated and stored in an environment free of dew condensation and these gases such as Hydrogen Sulphide, Hydrogen Sulphate, Chlorine, Ammonia and sulfur. 3) Avoid storing in sun light and falling of dew. 4) Do not use capacitors under high humidity and high and low atmospheric pressure which many affect capacitors reliability.
2	Circuit design ⚠ Caution	2-1 Operating temperature Operating temperature should be followed strictly within this specification, especially be careful with maximum temperature. 1) Do not use capacitor above the maximum allowable operating temperature. 2) Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitor will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product mounted on. Please design the circuit so that the maximum temperature of the capacitor including the self heating to be below the maximum allowable operating temperature. Temperature rise shall be below 20°C) 2-2 Operating voltage 1) Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V_{0-P} must be below the rated voltage. ——(1) and (2) AC or pulse with overshooting, V_{P-P} must be below the rated voltage. ——(3), (4) and (5) When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use a capacitor within rated voltage containing these irregular voltage.

Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage
Positional Measurement (Rated voltage)			

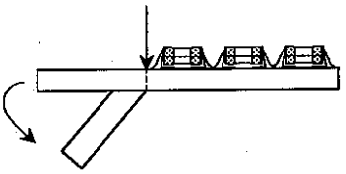
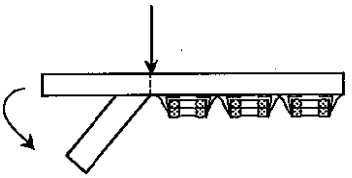
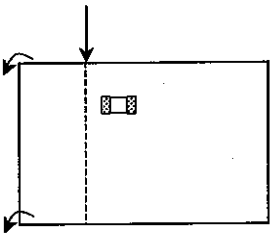
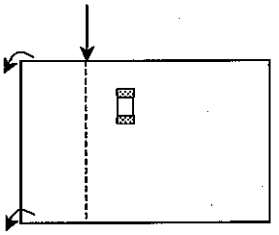
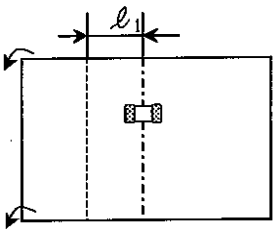
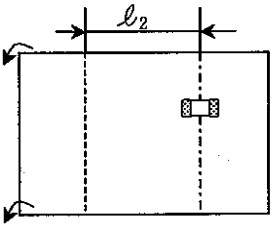
Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)
Positional Measurement (Rated voltage)		

2) Even below the rated voltage, if repetitive high frequency AC or pulse is applied, the reliability of the capacitor may be reduced.

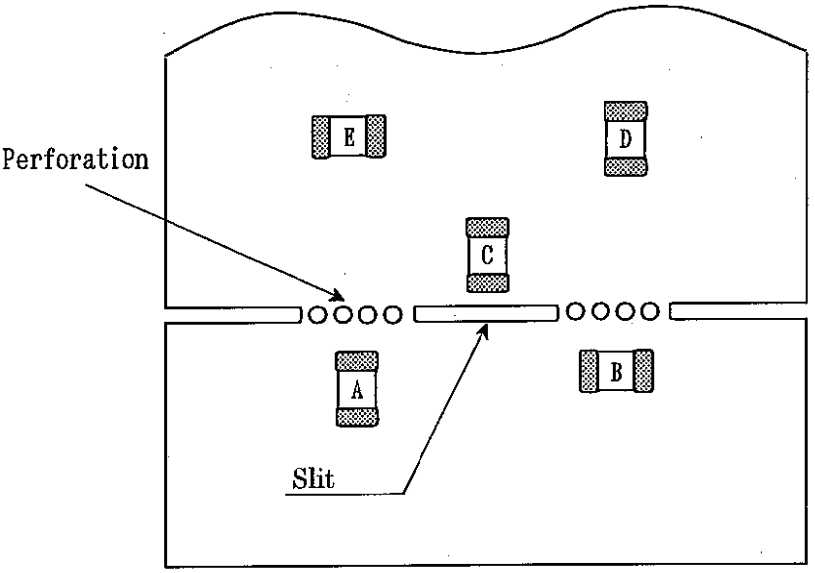
3) Voltage derating will greatly reduce the failure rate. Since the failure rate follows 3 power law of the voltage, the failure rate used under Uw with UR rated product will be lowered as $(Uw/UR)^3$.

No.	Process	Condition
3	Designing P.C.board	The amount of solder at the terminations has a direct effect on the reliability of the capacitor. 1) The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C.board, determine the shape and size of the solder lands to have proper amount of solder on the terminations. 2) Avoid using common solder land for multiple terminations and provide individual solder land for each terminations. 3) Size and recommended land dimensions.  (mm) Type / Symbol: CKG45N: A 3.3~3.7, B 1.2~1.5, C 2.7~3.2; CKG57N: A 3.9~4.3, B 1.5~2.0, C 4.5~5.0

No.	Process	Condition
3	Designing P.C.board	4) Recommended chip capacitor layout is as following.

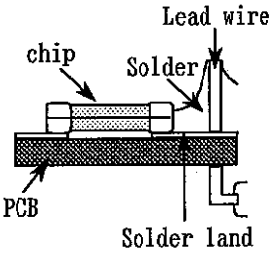
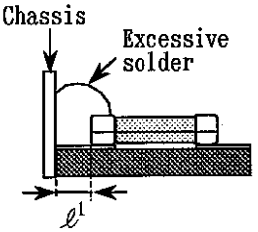
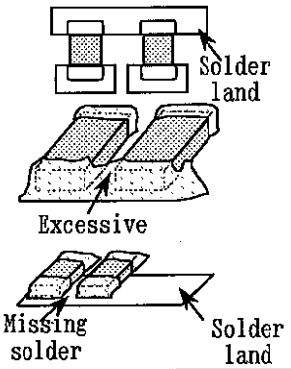
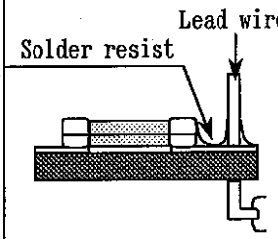
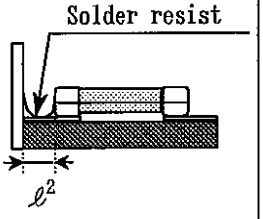
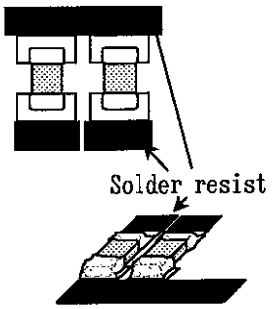
	Disadvantage against bending stress	Advantage against bending stress
Mounting face	Perforation or slit  Break P.C.board with mounted side up.	Perforation or slit  Break P.C.board with mounted side down.
Chip arrangement (Direction)	Mount perpendicularly to perforation or slit Perforation or slit 	Mount in parallel with perforation or slit Perforation or slit 
Distance from slit	Closer to slit is higher stress  $(\ell_1 < \ell_2)$	Away from slit is less stress  $(\ell_1 < \ell_2)$

No.	Process	Condition
3	Designing P.C.board	5) Mechanical stress varies according to location of chip capacitors on the P.C.board.

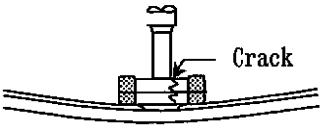
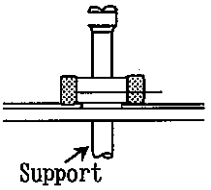
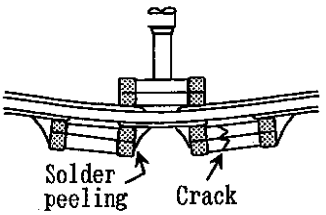
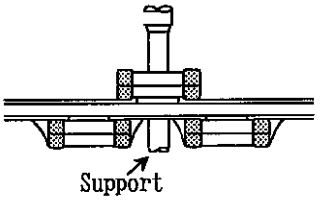


The stress in capacitors is in the following order.
A > B = C > D > E

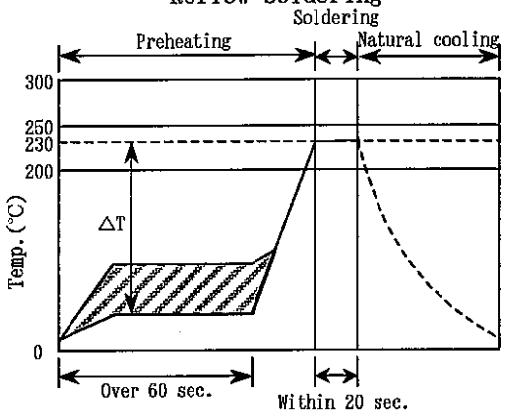
6) Layout recommendation

Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD
Need to avoid			
Recommendation			

No.	Process	Condition
4	Mounting	4-1. Stress from mounting head If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitor to result in cracking. Please take following precautions. 1) Adjust the bottom dead center of the mounting head to reach on the P.C.board surface and not press it. 2) Adjust the mounting head pressure to be 1 to 3N of static weight. 3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C.board. See following examples.

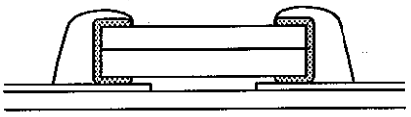
	Not recommended	Recommended
Single sided mounting		
Double-sides mounting		

when the centering jaw is worn out, it may give mechanical impact on the capacitor to cause crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.

No.	Process	Condition
5	Soldering	5-1. Flux selection Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended following. 1) It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended. 2) Excessive flux must be avoided. Please provide proper amount of flux. 3) When water-soluble flux is used, enough washing is necessary. 5-2. Recommended soldering profile by various methods Reflow soldering condition 1) Soldering condition (Pre heating temperature, soldering temperature and these times) is limited to reflow soldering method which is stipulated on the specification. 2) Chips should be mounted, shortly after a solder is on a P.C.Board. 3) Temperature differences (ΔT) ΔT : Temperature difference must be less than 130°C. Reflow soldering  4) Cooling condition Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference(ΔT) must be less than 100°C.

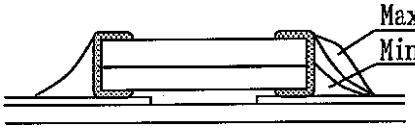
No.	Process	Condition
5	Soldering	5) Amount of solder Excessive solder will induce higher tensile force in chip capacitor when temperature changes and it may result in chip cracking. In sufficient solder may detach the capacitor from the P.C.board.

Excessive solder

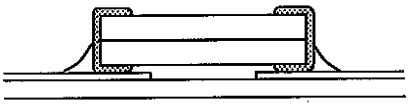


Higher tensile force in chip capacitor to cause crack

Adequate



Insufficient solder

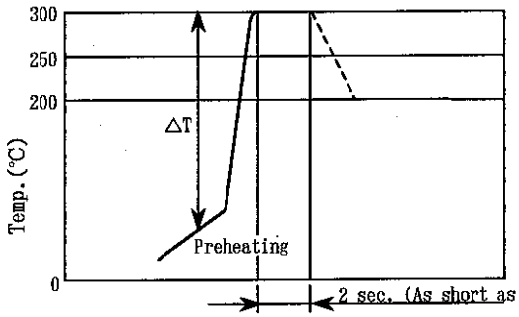


Low robustness may cause contact failure or chip capacitor comes off the P.C.board.

5-3. Solder repair by solder iron

1) Enough preheating is necessary to avoid chip cracking. Small temperature differences is less heat stress.
ΔT : Temperature difference must be less than 130°C.

Manual soldering
(Solder iron)



* Temperature of metal cap surface should not exceed 250°C.

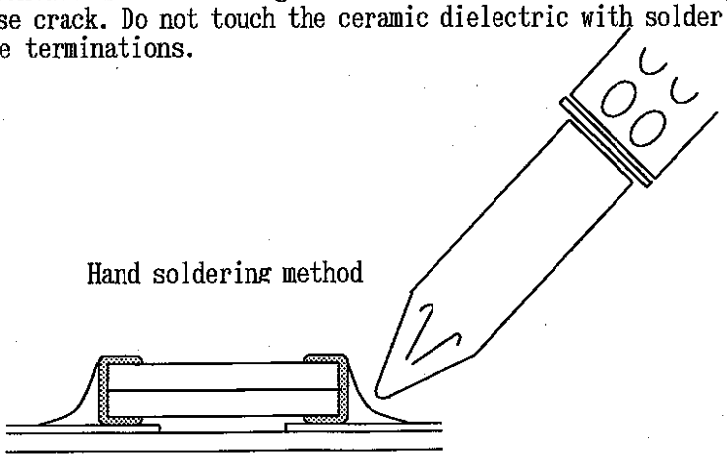
2) Selection of the soldering iron tip
Tip temperature of solder iron varies by its type, P.C.board material and solder land size. Higher the tip temperature , quick the operation is, but the heat shock may crack the chip capacitor. Following condition is recommended.

(Recommended solder iron condition)

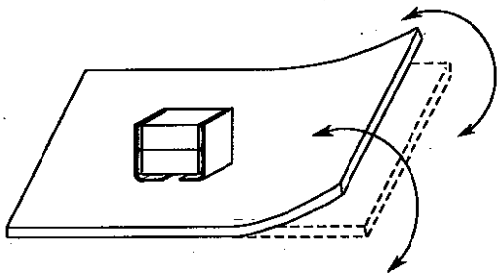
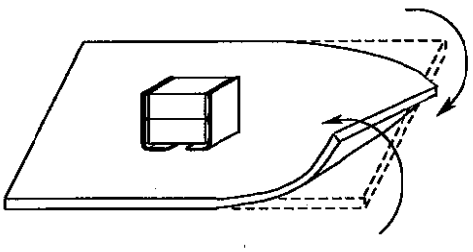
Temp. (°C)	Wattage (W)	Shape (mm)
300 MAX.	20 MAX.	φ3.0 MAX.

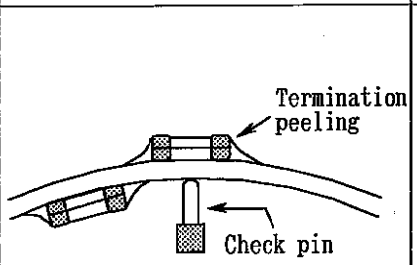
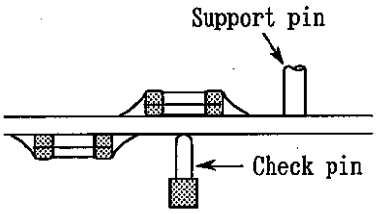
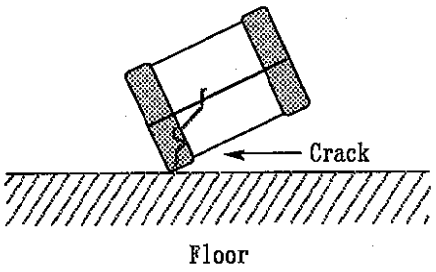
3) Direct contact of the soldering iron with ceramic dielectric of chip capacitor may cause crack. Do not touch the ceramic dielectric with solder iron other than the terminations.

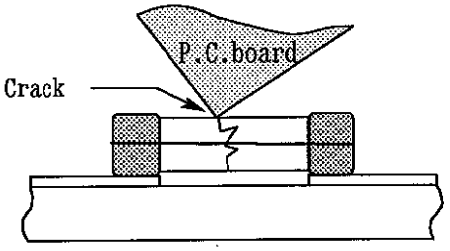
Hand soldering method



TDK

No.	Process	Condition
6	Cleaning	1) If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to chip capacitor surface to deteriorate especially the insulation resistance. 2) If cleaning condition is not suitable, it may damage the chip capacitor. 2)-1. Insufficient washing (1) Terminal electrodes may corrode by Halogen in the flux. (2) Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance. (3) Water soluble flux has higher tendency to have above mentioned problems (1) and (2). 2)-2. Excessive washing When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, following is the recommended condition. Power : 20W/ℓ max. Frequency : 40kHz max. Washing time : 5 minutes max. 2)-3. If the cleaning fluid is contaminated, density of Halogen increases, and it may bring the same result as insufficient cleaning.
7	Coating and molding of the P.C.board	1) When the P.C.board is coated, please verify the quality influence on the product. 2) Please verify carefully that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor. 3) Please verify the curing temperature.
8	Handling after chip mounted ⚠Caution	1) Please pay attention not to bend or distort the P.C.board after soldering in handling otherwise the chip capacitor may crack. Bend  Twist 

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>8</td><td>Handling after chip mounted
⚠Caution</td><td>2) When functional check of the P.C.board is performed, check pin pressure tends to be adjusted higher for fear of loose contact. But if the pressure is excessive and bend the P.C.board, it may crack the chip capacitor or peel the terminations off. Please adjust the check pins not to bend the P.C.board.
<table>
<tr><th>Item</th><th>Not recommended</th><th>Recommended</th></tr>
<tr><td>Board bending</td><td> 
</td><td> 
</td></tr>
</table></td></tr>
<tr><td>9</td><td>Handling of loose chip capacitor</td><td>1) If dropped the chip capacitor may crack. Once dropped do not use it. Especially, the large case sized chip capacitor is tendency to have cracks easily, so please handle with care.


2) Piling the P.C.board after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitor of another board to cause crack.

</td></tr>
<tr><td>10</td><td>Others⚠Caution</td><td>If a capacitor is failed in medical, aerospace or nuclear equipment, it may incur extensive loss of life and damage in society. For such purpose specially designed high reliability capacitor must be used. Please contact TDK in advance.</td></tr>
</table>

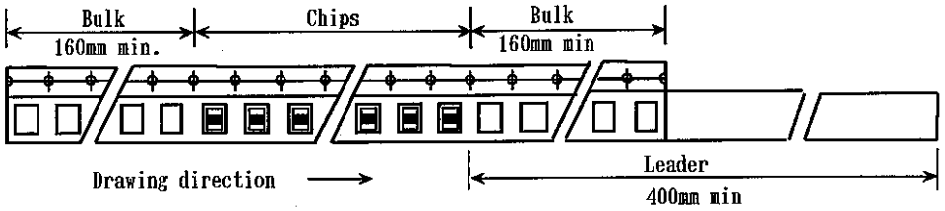
TAPE PACKAGING SPECIFICATION

TDK®

1. CONSTRUCTION AND DIMENSION OF TAPING

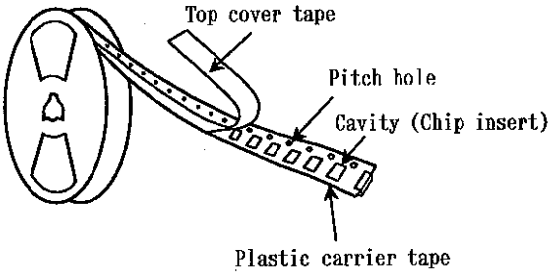
1-1. Dimensions of carrier tape
Dimensions of plastic tape shall be according to Appendix 3.

1-2. Bulk part and leader of taping



1-3. Dimensions of reel
Dimensions of ϕ330 reel shall be according to Appendix 4.

1-4. Structure of taping

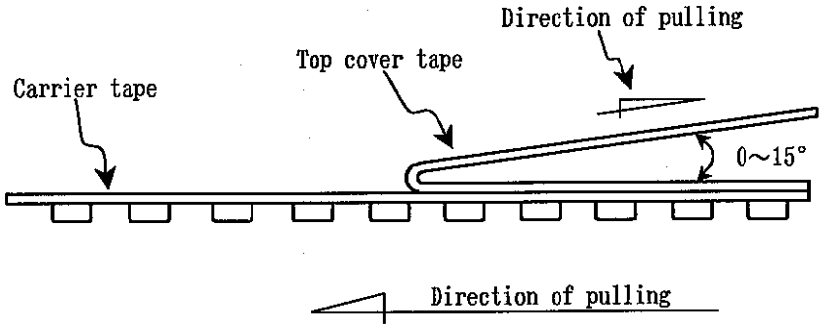


2. CHIP QUANTITY

Type	Thickness of chip	Taping Material	Chip quantity(pcs.)
			ϕ330mm reel
CKG45N	5.5 max.	plastic	1,000
CKG57N	5.5 max.		1,000

3. PERFORMANCE SPECIFICATIONS

3-1. Fixing peeling strength (top tape)
0.05-0.7N. (See the following figure.)



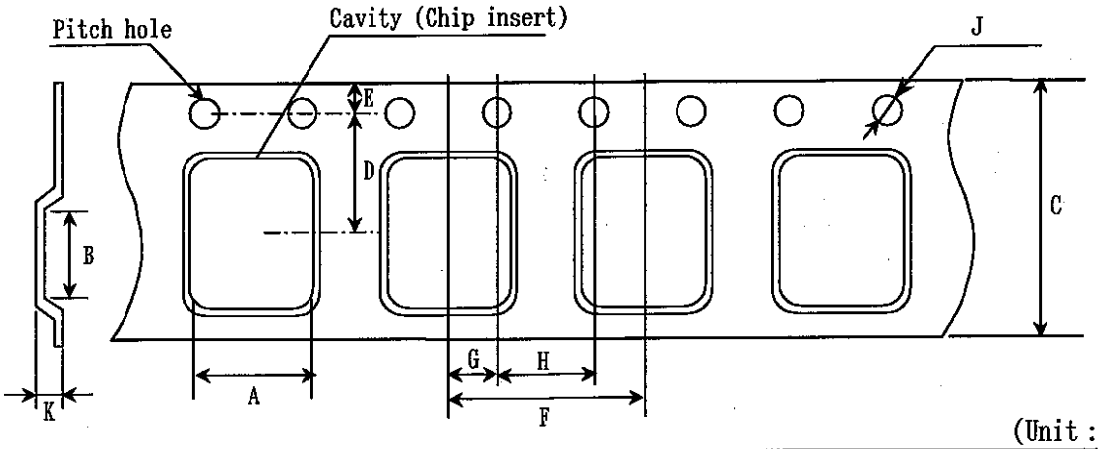
3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

3-3. The missing of components shall be less than 0.1%

3-4. Components shall not stick to fixing tape.

3-5. The fixing tapes shall not protrude beyond the edges of the carrier tape nor shall cover the sprocket holes.

Appendix 3 Plastic Tape



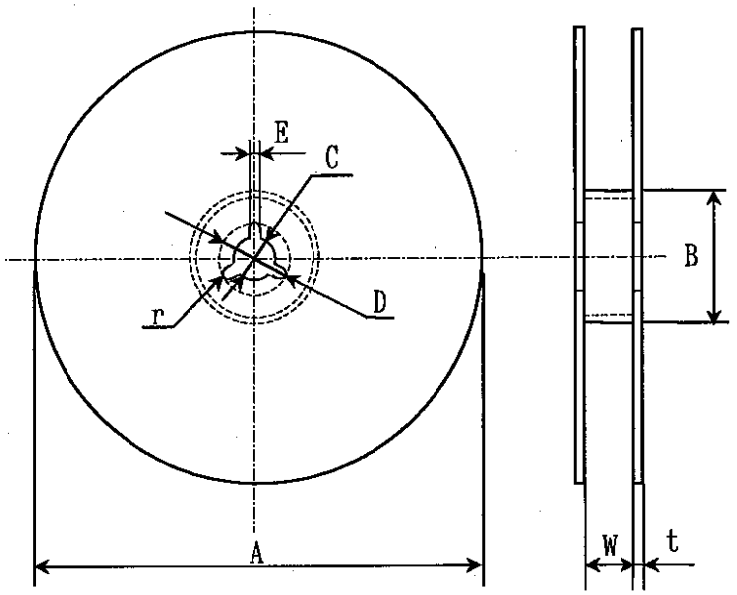
(Unit : mm)

記号 / 形名	A	B	C	D	E	F
CKG45N	(3.90)	(5.60)	12.0±0.30	5.50±0.10	1.75±0.10	8.00±0.10
CKG57N	(5.60)	(6.60)	16.0±0.30	7.50±0.10	1.75±0.10	8.00±0.10

記号 / 形名	G	H	J	K
CKG45N	2.00±0.10	4.00±0.10	$\phi 1.5^{+0.1}_{0}$	6.15 max.
CKG57N				

( ) : Reference value.

Appendix 4 Plastic Tape



(単位 : mm)

Symbol / Dimension	A	B	C	D	E	W
CKG45N	φ382 max.	φ50min.	φ13±0.5	φ21±0.8	2.0±0.5	13.5±1.5
CKG57N						17.5±1.5

Symbol / Dimension	t	r
CKG45N	2.0±0.5	1.0
CKG57N		