INTERCONNECT APPLICATION NOTE

STRADA Whisper 3.9mm Pair-In-Column(PiC) 85 Ohm Connector Standard Channel Daughtercard Routing Guide

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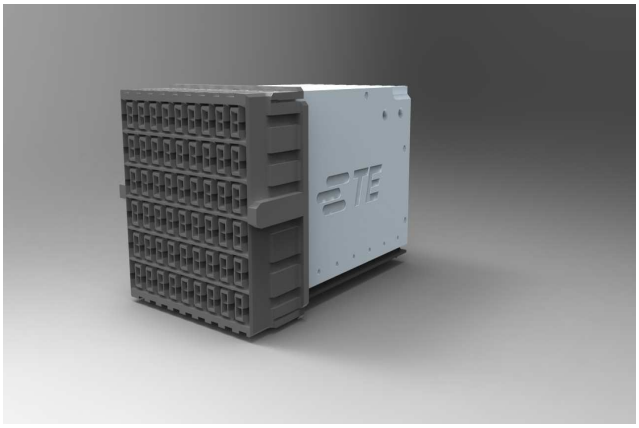

STRADA Whisper 3.9mm Pair-In-Column Connector

Table of Contents

STRADA Whisper PiC Connector Routing

I. INTRODUCTION

As engineers design systems that attempt to push serial speeds across backplane environments in the tens of gigabits per second range, the selection of the system's electrical connector becomes more significant. Electrical, mechanical, and manufacturing aspects of the connector must be considered simultaneously. At the board level these aspects combine with common board design practices to influence the design of the connector-to-board interface and how the board itself will be routed. The manner in which the connector is designed into the system can significantly impact the system's intended performance.

TE has been actively researching these areas in an effort to help customers use the STRADA Whisper connector in multi-gigabit serial systems. The combination of interconnect research and intimate knowledge of the connector is presented to provide insight into the capability of a STRADA Whisper-based system design. Furthermore, this document provides specific design recommendations that will address layout, electrical performance, and manufacturability tradeoffs of the connector at the board level.

II. CONNECTOR OVERVIEW: STRADA WHISPER

A. BACKGROUND

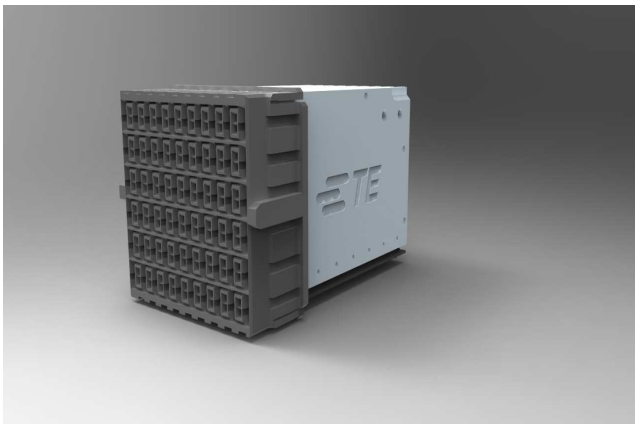

Figure 1: STRADA Whisper Pair-In-Column Connector

The STRADA Whisper connector is the first of the next generation of high speed backplane interconnects offered by TE. A revolutionary performance upgrade is a result of the extremely low noise characteristics of the individually shielded pairs which provide improved signal integrity and EMI performance over competitive products. The in-column pair orientation enables the STRADA Whisper connector to have low intra-pair skew due to skew compensation features incorporated in the connector design

1. FEATURES

- 56 Gb/s performance
- Individual shielded pairs facilitate excellent signal integrity and EMI performance
- Connector noise <1% @ 20 ps signal edge rate
- Connector insertion loss < 1.7dB and "flat" past 15 GHz
- Low Skew in-pair
- Optimized PCB footprint design
- A high degree of signal pair balance throughout the connector
- Daughtercard and Backplane use eye of needle (EON) press-fit technologies
- Compatible with existing card cage and connector mechanical envelopes
- Redundant points of contact in mating interface

2. APPLICATIONS

Designed for high speed or high signal quality applications that require serial data rates up to 40 Gb/s with superior signal integrity performance.

B. TYPICAL IMPLEMENTATIONS

1. RIGHT-ANGLE DIFFERENTIAL

STRADA Whisper is a high-speed connector that is typically implemented in differential applications. Although it can be implemented in single-ended applications as well, some additional grounding may be required depending upon the application. The variety of application spaces in which STRADA Whisper can be used are numerous, so the most common implementation space is described below.

STRADA Whisper is available in various pair count configurations. In this document the 6-pair configuration will be used as an example. For the 6-pair configuration each column contains six pairs in a 1.0" card-pitch module size. The connector has individually shielded pairs for excellent SI and EMI performance.

III. CONNECTOR DEFINITION

The following sections describe the STRADA Whisper daughtercard footprint. CAD models which include full mechanical dimensioning and tolerances are available for the STRADA Whisper connector and can be located at www.te.com. For overall dimensions, please refer to the latest customer drawings for the specific part that you are using. For other related usage information, please refer to the application specification for the STRADA Whisper product family.

A. DAUGHTERCARD FOOTPRINTS

Figure 2 depicts the dimensions of the via locations in the daughtercard footprint. The footprints shown include optimized antipads for 85Ω applications which will be described in greater detail later in this document.

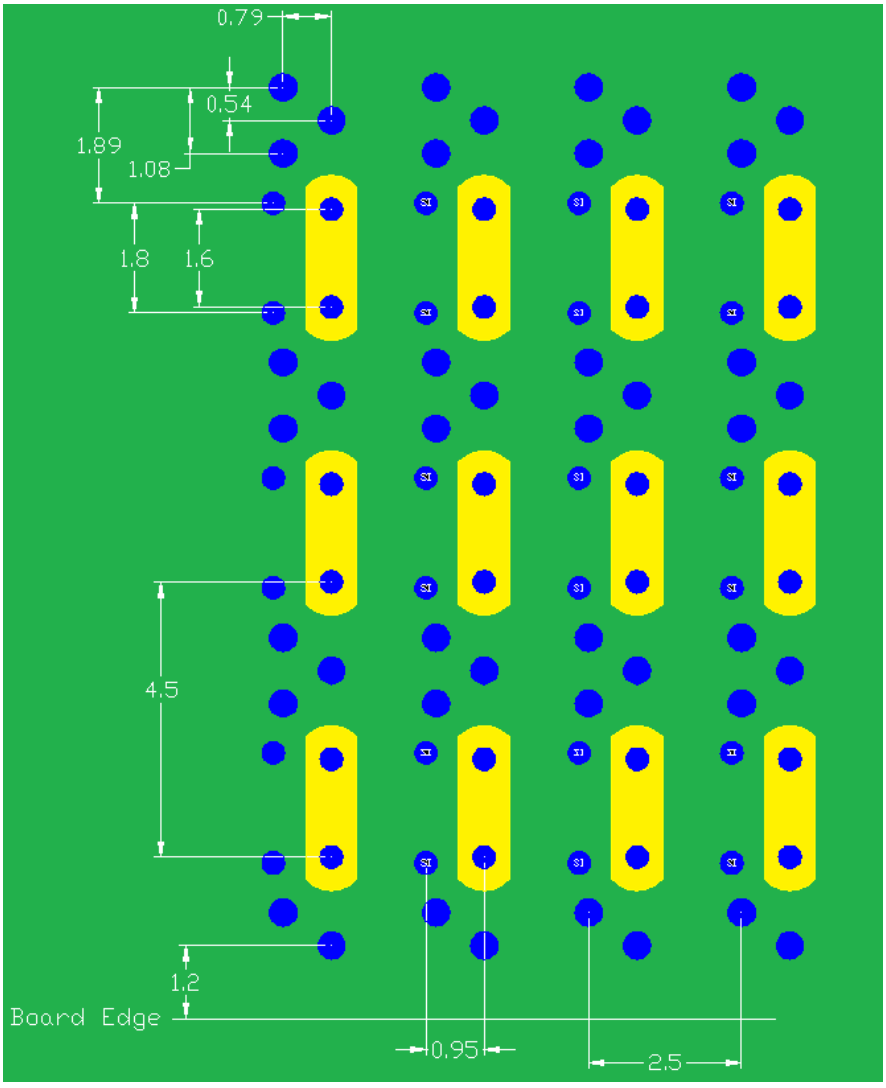

Figure 2: STRADA Whisper Daughtercard Footprint Dimensions

1. DRILLED HOLE DIMENSIONS

The dimensions critical to routing of the STRADA Whisper daughtercard connector are related to the hole pattern, or "footprint", of the connector. Table 1 is provided to quickly identify critical hole dimensions for the circuit board. These sizes may vary slightly depending on the surface finish as noted in the application specification. Table 1 provides typical hole size values. It is suggested to check with the intended PCB fabricator to ensure that the required drill sizes are procured prior to fabrication. Given today's PCB fabrication capabilities for aspect ratio (the thickness of the PCB divided by the smallest drill diameter) boards with aspect ratios higher than ~12:1 can limit the number of fabricators that can successfully build the PCB in volume production. For the Whisper daughtercard footprint, the signal drill hole size is 0.0145" and a 0.174" thick PCB would have a 12:1 aspect ratio.

Hole Dimension	Daughtercard Signal Hole Diameter mm (in.)	Daughtercard GND Hole Diameter mm (in.)
Drill Hole Size	0.368 ± 0.025 (0.0145 ± 0.001)	0.450 ± 0.025 (0.0177 ± 0.001)
Finished Hole Size	0.270 ± 0.04 (0.0106 ± 0.0016)	0.360 ± 0.04 (0.0142 ± 0.0016)
Copper Thickness Min.	0.0254 (0.001)	0.0254 (0.001)

Table 1: Daughtercard Connector Hole Dimensions

2. FABRICATION TECHNOLOGY

Other important dimensions for board layout are also determined by the capabilities of the circuit board fabricator. Current high-tech PCB industry fabrication technology (i.e. capability) requires minimum pad sizes ranging from D+8 mils through D+16 mils, where "D" is the diameter of the drilled hole size (1 mil, or 0.001", is 0.0254 mm). The resulting pad size for a given technology is typically defined as the minimum pad size required to maintain 0.05 mm (0.002") of annular ring for a given PCB manufacturer's capability. Annular ring is an industry standard measure of the clearance between the pad edge and worst-case drill edge after manufacturing. For the STRADA Whisper daughtercard footprint this requirement results in minimum pad sizes ranging from 0.571 mm (0.0225") to 0.774 mm (0.0305"). Because STRADA Whisper is typically used in high speed or dense applications where routing issues are most significant, *it is recommended that all pad dimensions be no larger than D+10 mil*. The pad diameter may be optimized for specific project needs, and should be evaluated on a project and vendor basis. Designing with a D+8 mil technology PCB or smaller will improve electrical performance, but could mean reduced yields or breakout, potentially adding cost to the PCB or violating industry specification compliance. Designing with a larger than D+10 mil pad size reduces electrical performance by increasing the capacitance of

the plated through-hole to nearby pads, vias and traces. Where possible, the largest *appropriate* pad size should be used to provide the PCB manufacturer with the greatest flexibility, thereby reducing overall system costs as long as it meets the performance requirements of the system.

Note: The remainder of the document will assume a D+10 mil fabrication technology and a minimum pad to trace clearance of 0.127 mm (0.005") for calculating routing dimensions.

a. PAD SIZE

A 0.622 mm (0.0245") diameter pad should be used with all STRADA Whisper daughtercard connector internal signal layers. For higher-tech PCBs (D+8 mil), the pad would be 0.571 mm (0.0225”). A D+6 mil or 0.520mm (0.0205”) pad is recommended on external layers. Table 2 summarizes different pad sizes for different manufacturing capabilities.

	Internal Layer Pad Size				
	High-tech ◄				► Low tech
	D+8	D+10	D+12	D+14	D+16
DC Connector Pins Signal	0.571mm (0.0225”)	0.622 mm (0.0245”)	0.673 mm (0.0265”)	0.724 mm (0.0285”)	0.774 mm (0.0305”)

Table 2: Pad sizes for STRADA Whisper Connector

b. NON-FUNCTIONAL PADS

The removal of non-functional internal pads will improve signal integrity and manufacturability of the PCB. However, some assembly facilities prefer that unused pads are retained in order to maintain hole integrity through various soldering processes. For electrical reasons it is recommended that unused pads be removed on internal layers. Additionally, landless pads (D+6 mil or smaller) are recommended for external layers that do not have signal connections to the connector pad.

c. THERMAL RELIEFS

Thermal reliefs are not required on ground or power pins, because the STRADA Whisper connector uses a press-fit technology. A direct connection to reference and power planes will offer the lowest inductance connection to the circuit board.

d. ANTIPAD SIZE

Antipads, or plane clearances (Figure), are required to separate signal holes from reference voltages to avoid shorting. Choosing the proper size of these clearances is critical in determining several other design

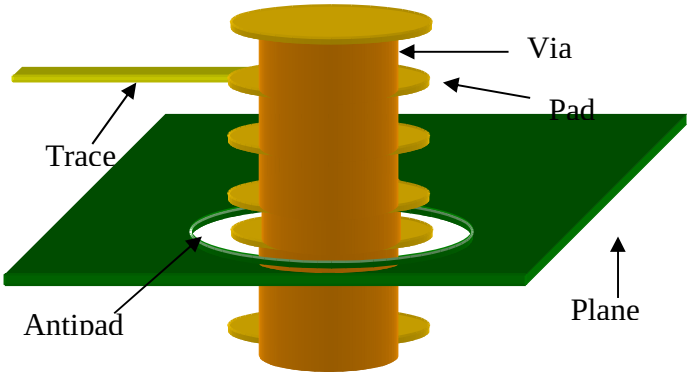

Figure 3: Antipad Illustration

parameters: signal integrity, EMI, voltage breakdown, and manufacturability.

Determining the proper antipad size for STRADA Whisper depends upon system design goals. Several scenarios are described below.

Antipad sizes are minimized:

- To reduce noise by closely shielding adjacent pins with reference planes
- To reduce EMI by minimizing aperture sizes in reference planes
- To maintain a strong reference to ground for single-ended traces and ground referenced differential traces

Antipad sizes are maximized:

- To maximize voltage breakdown spacing between the pin and the reference plane
- To increase manufacturability by reducing the chance of shorting.
- To reduce reflections in a high-speed gigabit serial system by reducing the capacitive effect (if present) of the plated through-hole.

In cases where antipads are minimized, the recommended antipad size is the pad diameter plus 0.254 mm (0.010”). This size maximizes trace coverage, while not risking shorting the plane to the barrel in the case of drill breakout. Using a minimal antipad will increase the capacitance of the via and could degrade system performance at high speeds.

When antipads are maximized, the antipad geometry is dependent on the type of signals passing through the vias.

The suggested antipad structure for differential signals encompasses two adjacent signal vias. This structure minimizes the via capacitance for both vias, while maintaining coupling between the two signals within the differential pair. The recommended antipad is designed to balance routable trace widths and associated ground coverage with the minimization of via capacitance.
The antipad geometry may be adjusted to further optimize both, once a design specific trace geometry and fabrication technology is determined.

Figure 4 details the recommended antipad dimensions for the daughtercard connector. These resulting antipad dimensions of 2.70mm (.1063”) x 0.83mm (.0327”) represent a geometry which maximizes routable trace widths and associated ground coverage. The daughtercard antipad size should not be increased above the specified values, otherwise the footprint impedance is likely to exceed 85Ω. Routing geometries that are achievable with this geometry are discussed further in section IV.

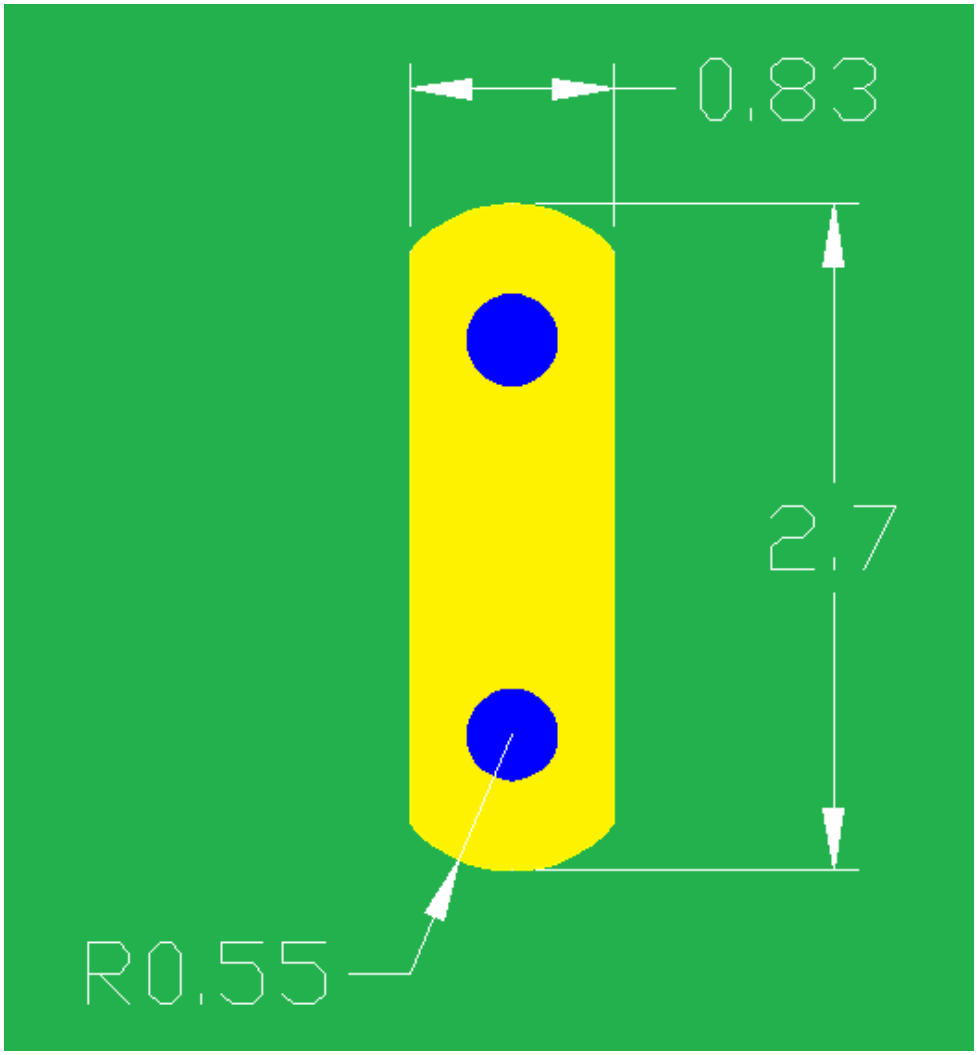

Figure 4: Daughtercard Antipad Geometry

Figure 5 and Figure 6 outline breakout antipads to be used only on layers adjacent to the breakout layer. Each diagram shows representative routing to be used in conjunction with the defined antipad.

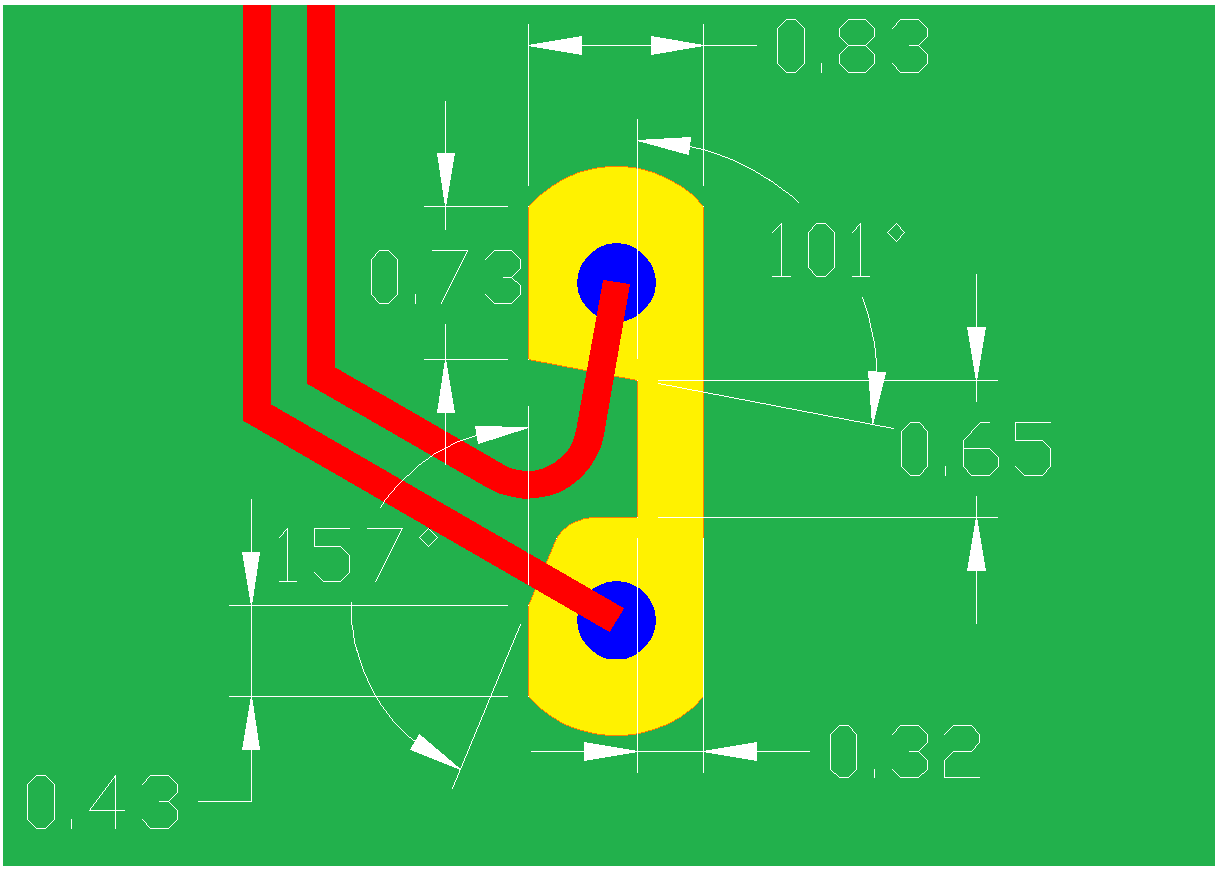

Figure 5: Daughtercard Breakout Antipad, Left-Side

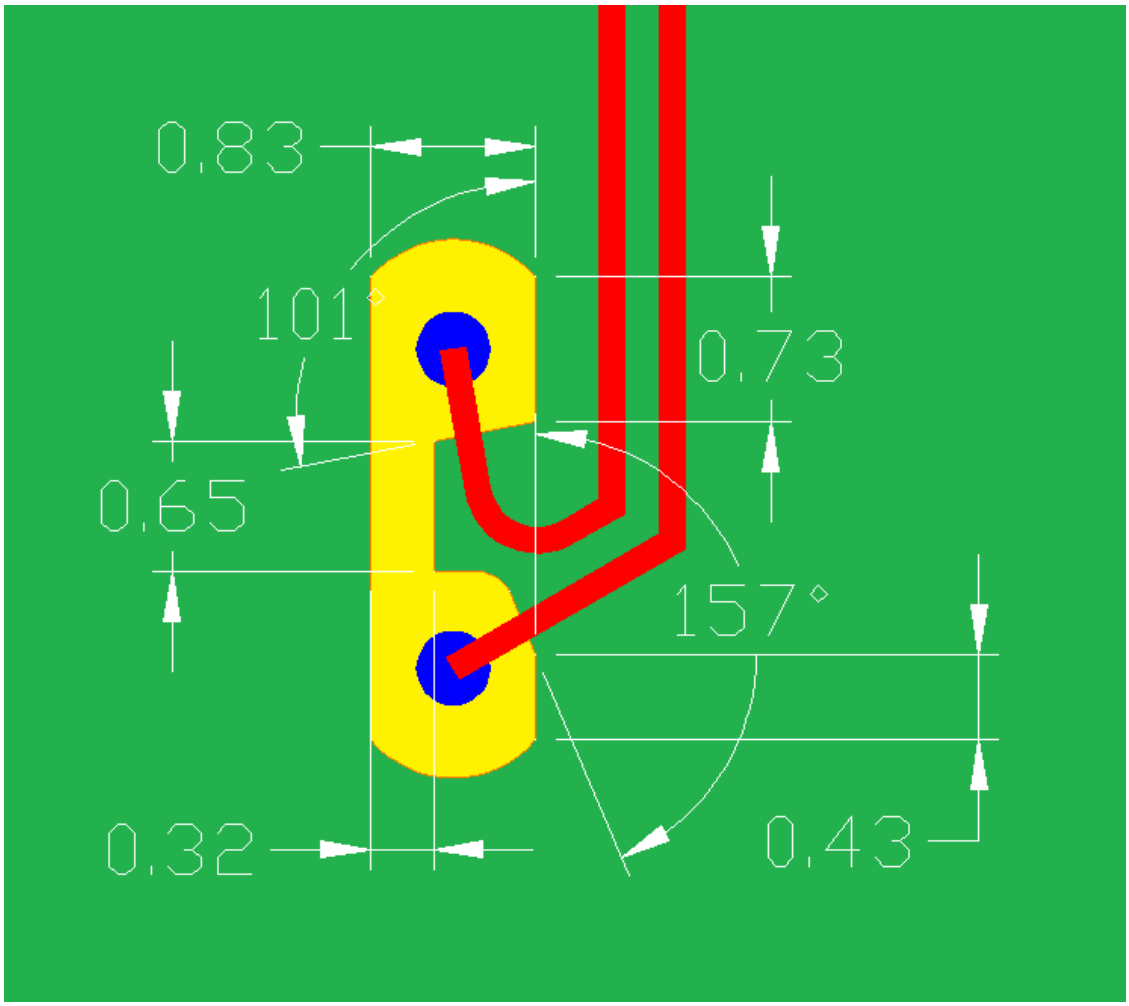

Figure 6: Daughtercard Breakout Antipad, Right-Side

The recommended antipad size on power planes should be the same or greater than the antipads on the ground planes. However, if the planes are hazardous high voltage power, noisy, or are tightly spaced with small dielectrics separating the planes it is recommended to completely remove the planes within the connector pinfield.

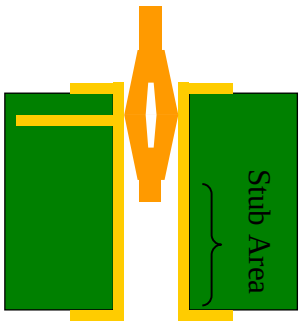

Figure 7:Via Stub

3. HIGH SPEED VIA DESIGN

At gigabit speeds, one of the limiting factors in system design is the effect caused by the via stub in the board. A via stub is the portion of the via that is not in series with the transmission path of the signal, as shown in Figure7. At high frequencies, this parallel path creates a

significant capacitive discontinuity, which degrades the throughput of the link. Although it has a small impact at lower frequencies, this stub typically becomes critical at speeds greater than 3.125 Gbps.

STRADA Whisper was designed to allow for various techniques to be applied to treat the via and remove the stub, without impacting the press-fit contact in the hole. When the connector is fully seated, the bottom tip of the eye of needle (EON) pins and the micro-action pin (MAP) tails extend slightly beyond 1.0 mm (0.039") into the hole. Because the connector only requires 1.0mm (0.039") of via length, beyond that depth, various techniques can be employed to modify the via to eliminate the stub. Consult your board fabrication facility regarding their capabilities for these techniques.

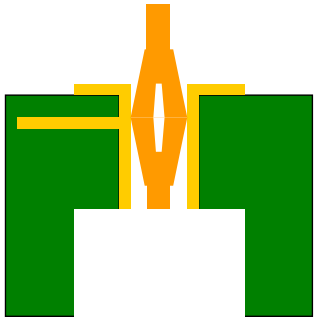

Figure 8: Counterbored Via

a. COUNTERBORING (I.E. BACKDRILLING)

Counterboring is a technique that has been used for years by the microwave industry to treat vias in microwave designs. With digital signaling approaching microwave frequencies, similar techniques can be employed to enhance the signal integrity of a link. Counterboring is performed as one of the final steps in the board manufacturing process. After the multilayer board is laminated, drilled, and plated, designated holes are control-depth drilled to remove any via stub that is present. This controlled-depth drill should allow a minimum length of barrel to remain in the hole to allow the eye-of-needle to engage the via. Figure 8 illustrates a counterbored via. The minimum remaining via depth (after counterboring) is 1.0 mm (0.039") for both the EON and MAP pins. For routing that occurs on layers above this minimum, a stub will exist and will degrade the throughput of the link.

b. BLIND VIAS

An alternative approach that is equally as effective as counterboring is the use of blind vias. Like counterboring, care must be taken to ensure that the depth of the blind via is sufficient to fully engage the eye-of-needle and accommodate the entirety of the pin tip. Due to the additional operations needed in manufacturing for blind vias manufacturing costs will be higher than a typical multilayer board with the same number of layers. Care should be taken to ensure successful cleaning of the via such that long-term reliability is maintained. Figure 9 illustrates a blind via. Consult Product Engineering for via depth guidance.

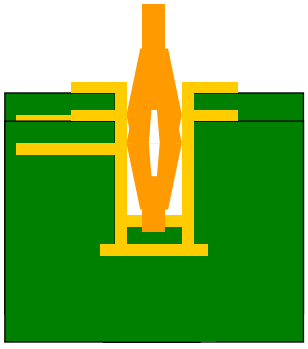

Figure 9: Blind Via

IV. ROUTING

The STRADA Whisper connector can be used for both single-ended and differential signals, however only the more common routing of differential signals will be examined.

A. DAUGHTERCARD ROUTING

1. ROUTING CHANNELS

The connector's routing channel is defined by the space between adjacent vias in the connector pinfield that is available for trace routing. Typical routing is implemented vertically (between columns of vias), as shown in Figure 10. With a D+10 mil pad size, the remaining space easily allows for 5-mil differential lines with 7-mil intra-pair spacing. In board materials with dielectric constant values in the 3 to 4 range, these geometries will provide well matched common and differential impedances in typical board stackups. These differential trace geometries also allow for a 12.5-mil antipad to trace clearance and an 8-mil ground drill to trace clearance. Although larger differential geometries will fit within the routing channel, care should be taken if increasing the overall differential pair width beyond 25mils due to manufacturing tolerances that could effect electrical performance. When using pair geometries smaller than the above examples, it is advised to bias the pair away from the antipad (not centered in the channel), while maintaining recommended spacings to the column of ground vias that is shared between adjacent routing channels.

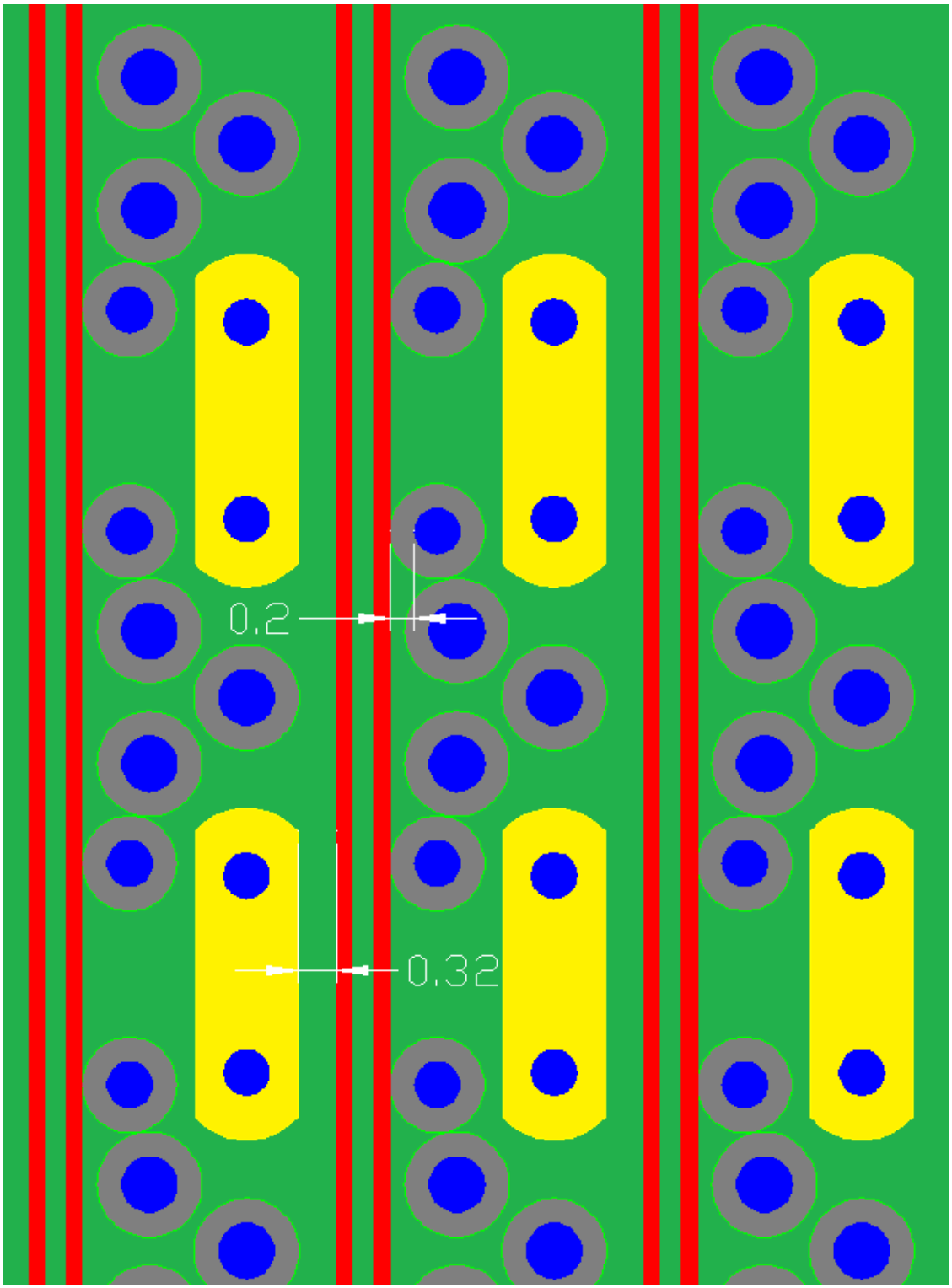

Figure 10: Daughtercard Channel Routing with 5-7-5 trace

2. ESCAPE ROUTING

The recommended escape routing from the connector pin has been designed in a way that results in zero skew in the differential trace. Figure 11 illustrates the escape routing for a differential pair consisting of signal vias marked as 1 and 2. Escape routing for via 1 runs from point A (on its corresponding pad) to point B. Similarly, escape routing for via 2 runs from point C on its pad to point D. Notice that point B and D coincide with a straight reference line passing through the center of the signal via farthest from the board edge. The physical route length of the trace between point A and B should be equal to the physical length of the trace between point C and D.

The initial width, starting at the via, of the escape traces between A and B as well as between C and D, should remain the same width as differential trace width, no single-ended breakout trace width compensation is needed. At no point should any portion of the trace pair have a spacing smaller than the differential spacing. Since the physical length of the differential traces beyond points B and D are equal, having ensured equal length escape traces between point A and B and between point C and D, ensures that the overall routing from a via pair to the destination via pair is electrically skew-less.

As with all routing, escape traces should maintain a minimum manufacturing distance between trace edges and ground vias of 0.2032mm (.008”).

As mentioned in Section III.A.2.d, it should be noted that antipad reduction is necessary for the daughtercard footprint only on the layers above and below the layer where traces escape from the footprint vias, to provide ground coverage for the trace between point A and B.

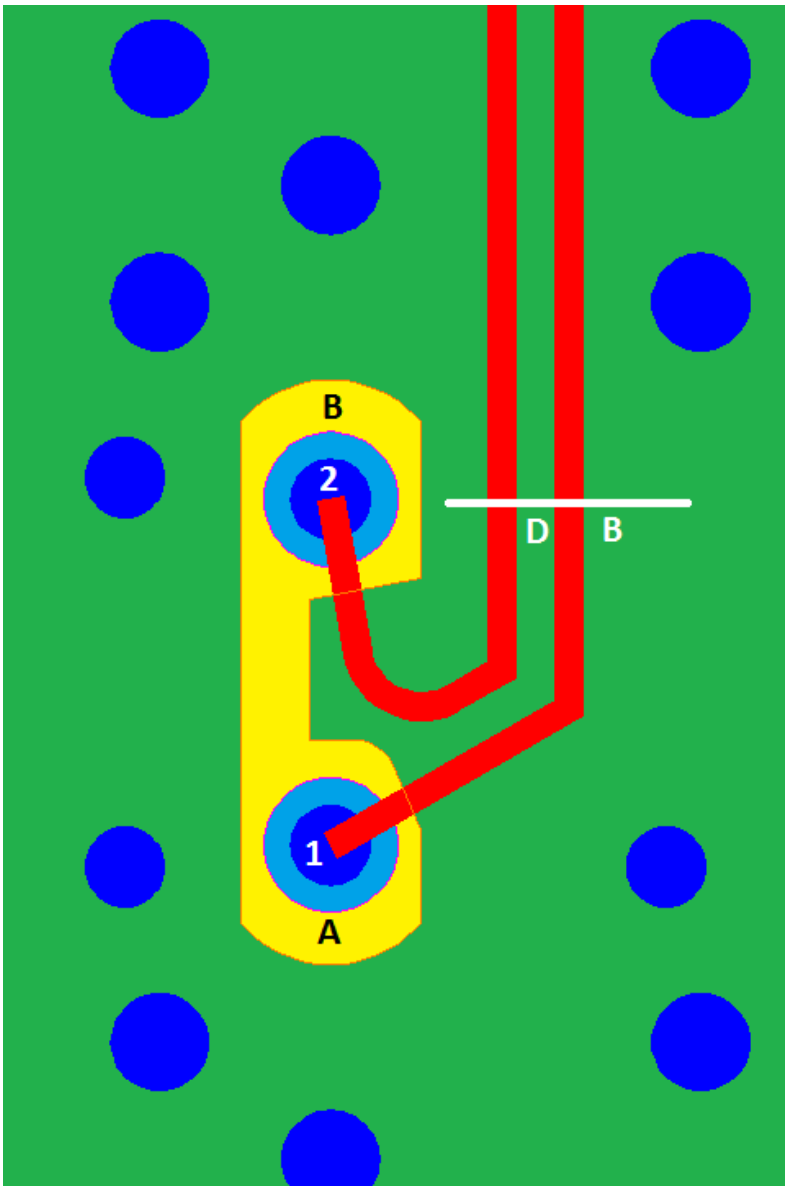

Figure 11: Example Breakout

3. LAYER COUNT ANALYSIS

Figure 12 illustrates the typical routing technique for the 6-pair daughtercard connector. Typically the 6-pair connector is routed in 6 layers. By allowing routing out the end of the connector footprint, the layer count can be reduced. Antipad reductions, shown in the vertical routing technique, are only necessary on layers above and below trace routing to avoid an inductive breakout.

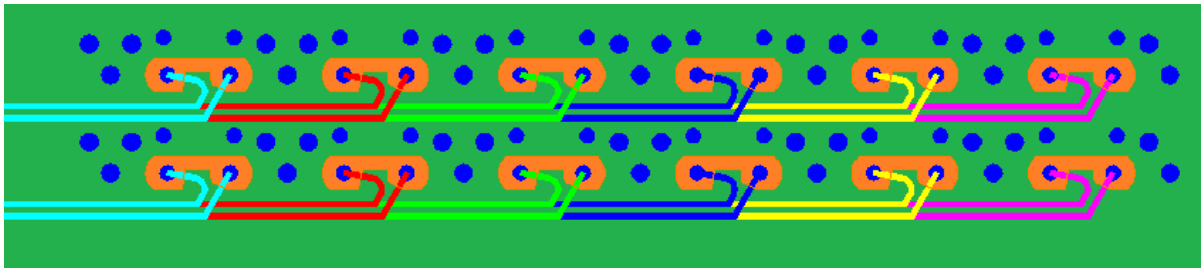

Figure 12: Typical Layer Count Breakdown for 6-pair Daughtercard Connector

4. LAYER SPECIFIC ROUTING

Layer Specific Routing (LSR) is the use of a specific routing layer for each connector pair based upon performance criteria. It is recommended to implement LSR in order to reduce far end crosstalk in the via field. When counterboring or other stub removal techniques are used, this configuration reduces the amount of coupling of each signal via to its neighboring signals. Table 3 shows an example of LSR configurations for the daughtercard connector when 6 routing layers are available. The value within the table represents the routing layer upon which each pair should reside. Nine columns of the connector are shown for reference, but the pattern continues for additional columns of the connector.

	A	B	C	D	E	F	G	H	J
17/18	1	1	1	1	1	1	1	1	1
14/15	2	2	2	2	2	2	2	2	2
11/12	3	3	3	3	3	3	3	3	3
8/9	4	4	4	4	4	4	4	4	4
5/6	5	5	5	5	5	5	5	5	5
2/3	6	6	6	6	6	6	6	6	6

Table 3: 6-layer LSR Recommendation for 6-pair Daughtercard Connector

V. GENERAL

A. PINOUT RECOMMENDATION

In order to reduce noise within the connector pinfield, an interstitial transmit and receive pin assignment is recommended. An interstitial pin assignment, similar to a checkerboard pinout, is an alternating pattern of transmit and receive signals as shown in Figure 13.

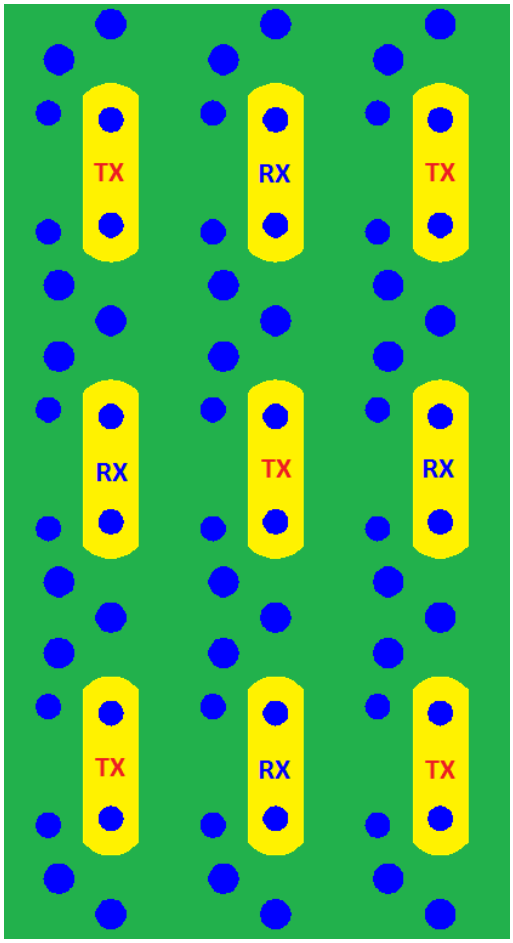

Figure 13: Interstitial Pinout

B. EXAMPLE STACKUPS AND MATERIAL CHARACTERISTICS

The stack heights and material properties shown in Figure5 and **Error! Reference source not found.**6 were used to achieve 85Ω impedances for the 5-7-5 channel and escape routing scenarios illustrated in Section IV.

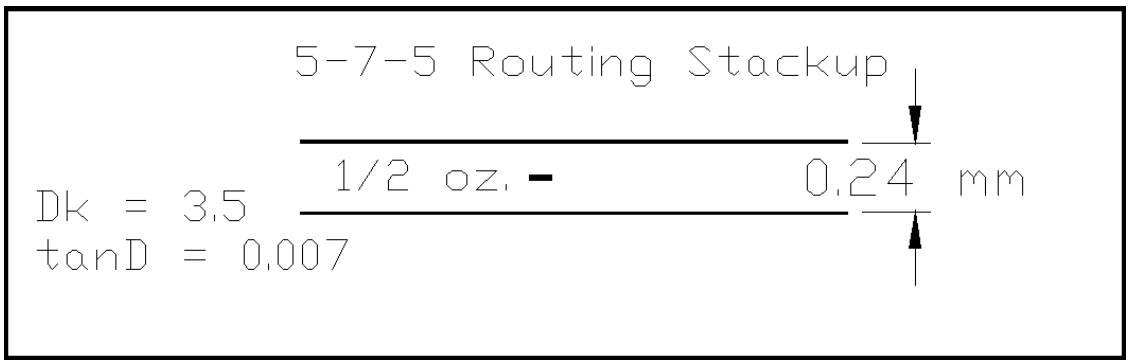

Figure 14: 5-7-5 Routing

C. Recommended Routing Techniques

1. Right-angle Bends

It is recommended to avoid using right-angle bends (90°). Use of two 45° bends or filleted corners is recommended. Less sharp turns will minimize the impedance discontinuity resulting in a reduction of reflection on the signal at the bend.

VI. Part Placement

Part placement and spacing guidelines as well as associated up-to-date mechanical dimensions should be obtained in addition to this document. Placement related information is contained within the application specification, document #114-13282. The full mechanical dimensioning and tolerances are available for all versions of the STRADA Whisper connector within the customer drawing for the specific part number of interest. All of this information can be found at www.te.com, and also by contacting either your local TE sales support or the appropriate contact listed below in Section VIII.

VII. Additional Information

A. Gigabit Research and General Application Notes

More information regarding TE research into the transmission of electrical signals at gigabit speeds or general application notes is available for download at www.te.com/products/simulation.

B. Electrical Models

Electrical S-parameter models and Allegro Footprints for the STRADA Whisper may be requested at modeling@te.com.

C. WEBSITE

More information regarding the STRADA Whisper connector can be found on the web at www.te.com/products/stradawhisper

VIII. CONTACT INFORMATION

The following contact can be used to obtain additional information on the STRADA Whisper product family and other connector related issues.

Technical Support Center	1-800-522-6752	www.te.com/help