DATASHEET

CP2000AC48TEZ-FB2 Compact Power Line High Efficiency Rectifier

Input: 100 – 120/220 – 240 V_{AC}; Output: 2250W @ 48V_{DC}; 5 V_{DC} @ 4W

RoHS Compliant

The CP2000AC48TEZ-FB Rectifier has an extremely wide programmable output voltage capability and fold-back current limiting features. High-density front-to-back airflow is designed for minimal space utilization and is highly expandable for future growth. This custom rectifier incorporates both RS485 and dual-redundant I^2C communications busses that allow it to be used in a broad range of applications. Feature set flexibility makes this rectifier an excellent choice for a set of applications requiring operation over a wide output voltage range.

Applications

- Wide band power amplifiers

Features

- Efficiency 95%
- Compact 1RU form factor providing 30 W/in^3
- 2250W @ 52V from nominal 220 – 240V_{AC}
- 1200W from nominal 100 – 120V_{AC} (for Vo > 30V_{DC})
- Output voltage programmable from 18V – 58V_{DC}
- PMBus compliant dual I^2C and RS485 serial busses
- Power factor correction (meets EN/IEC 61000-3-2 and EN 60555-2 requirements)
- Output overvoltage and overload protection
- AC Input overvoltage and undervoltage protection
- Over-temperature warning and protection
- Redundant, parallel operation with active load sharing
- Redundant +5V Aux power
- Remote ON/OFF
- Hot insertion/removal (hot plug)
- Four front panel LED indicators
- UL* Recognized to UL60950-1, CAN/ CSA† C22.2 No. 60950 -1, and VDE‡ 0805-1 Licensed to IEC60950-1
- CE mark meets 2006/95/EC directive§
- Internally controlled Variable – speed fan
- RoHS Directive 2011/65/EU and amended Directive (EU) 2015/863
- Special Foldback Curve

* UL is a registered trademark of Underwriters Laboratories, Inc.
† CSA is a registered trademark of Canadian Standards Association.
‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.
§ This product is intended for integration into end – user equipment. All the required procedures for CE marking of end – user equipment should be followed. (The CE mark is placed on selected products.)
** ISO is a registered trademark of the International Organization of Standards.

Technical Specifications

Electrical Specifications

Input

Parameter	Min	Typ	Max	Units	Notes
Startup Input Voltage					
Low – line Operation			90		
High – line Operation			200		
Operating Voltage Range				V_{AC}	
Low – line Configuration	90	100, 110, 120	140		
High – line Configuration	200	220 – 240	265		
Surges (no damage)	305				
Input Frequency	47		66	Hz	
Input Current			12 13.5	A	At 110 V_{AC} At 240 V_{AC}
Inrush Transient		25	30	Apk	Measured at 25°C for all line conditions; does not include X-Capacitors charging.
Input Leakage Current		2.5	3.5	mA	Measured at 265V_{AC}, 60Hz
Power Factor	0.96	0.98			From 50% to 100% (2250W @ HL, 1200W @ LL) load
Efficiency[1] 30 – 90% of FL	93	95		%	With or'ing function, aux 5V output, dual/redundant I^2C and RS485 communications and POE isolation >30% load Test condition: input; 240V_{AC}, 60hz, output; 52V_{DC}
Efficiency[1] >38V	85			%	
Holdup		20 30		ms	48V_{DC}, Measurement starts at zero crossing of the ac voltage, and voltage decayed to 40V. For loads below 1200W.
Ride thru	1/2	1		cycle	Tested at nominal 115V and 230V. Complies to CISPR24 standards
Power Fail Warning[2]	3	5		ms	Alarm issued via PFW signal going LO 5 ms prior to the main output decaying below 40V_{DC}.

Main Output

Parameter	Min	Typ	Max	Units	Notes
Output Power	1200 2250			W	Above 30V_{DC} from nominal 90 – 120V_{AC} upto 55°C. Above 48V_{DC} from nominal 200 – 265V_{AC} upto 55°C
Default Set point		48		V_{DC}	Output floats with respect to frame ground.
Overall Regulation[3]	-1 -2		+1 +2	%	0 – 45°C, minimum load 2.5A > 45°C
Output Voltage Set Range	18		58	V_{DC}	Analog margining and RS485
	18		58	V_{DC}	Set by I^2C
Output current	1 1		23 43.3	A	1200W @ 52V @ 90 – 120V_{AC}. 2250W @ 52V @ 200 – 240V_{AC}.
Current Share V_o >42V V_o <42V	 -5 -10		 5 10	%FL	Compared to the average output current delivered by a set of Rectifiers. Loads > 50% FL
Output Ripple RMS (5Hz to 20MHz) Peak-to-Peak (5Hz to 20MHz)		 60	 100 500	 mV_{rms} mV_{p-p}	Measured with 20MHz bandwidth under any condition of loading. Minimum load is 1A
External Bulk Load Capacitance	0		5000	µF	External capacitance can be increased but the rectifier will not meet its turn – ON rise time requirement.
Turn – on Delay Rise Time – Standard (PMBus) – Telecom (RS485)[4] Overshoot		 5 100 5	 2	 s ms s %	Monotonic Turn_On from 30% to 100% of Vnom above -5°C operation. Monotonic Turn_On from 60% to 100% of Vnom below -5°C operation.
Load Step Response ΔI ΔV Response Time		 2.0 2	 50 	 %FL V_{DC} ms	 ΔI/Δt slew rate 1A/µs. Settling time to within regulation requirements. Minimum load of 2.5 amperes required.

[1]At 52V_{DC}, 240V_{rms} and 25°C.
[2]Internal protection circuits may override the PFW signal and may trigger an immediate shutdown.
[3]Includes all variations due to specified load range, drift, and environmental conditions.
[4]Below -5°C, the rise time is approximately 5 minutes to protect the bulk capacitors.

Technical Specifications (continued)

Electrical Specifications (continued)

Main Output (continued)

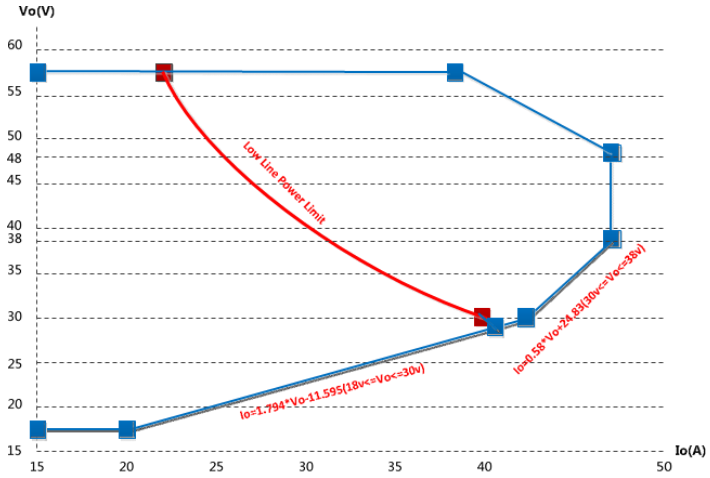
Parameter	Min	Typ	Max	Units	Notes
Power limit – high line	2250			W	
Power limit – low line	1200			W	

The overload current limit threshold should be set ≅ 5% above the load envelope shown here

High Line

Vo(V)	18	20	23	25	28	32	36	38	48	50	53	56	58	
Io(A)	20.7	24.3	29.7	33.3	38.6	43.4	45.8	46.9	46.9	45	42.5	40.2	38.8	

Permissible Load Boundary



Low Line

Vo(V)	18	20	23	25	28	32	36	38	48	50	53	56	58	
Io(A)	20.7	24.3	29.7	33.3	38.6	37.5	33.3	31.6	25	24	22.6	21.4	20.7	

Contract terms are for supporting all loads inside the load map. The customer will develop a control interface which maintains the operating voltage and current so as to not exceed the load map.

System Power Up: Units should be able to be plugged in one at a time and guarantee system start up. Units should stay in current limit for approximately 20 seconds to guarantee restart.

Over – voltage				
Delayed		60	V_{DC}	200msec delayed shutdown to be implemented.
Immediate Latchoff		65	V_{DC}	Instantaneous shutdown above this point.
	Three restart attempts may be implemented within a one minute window prior to a latched shutdown			
Over – temperature				
Warning		5	°C	Implemented prior to commencement of an OT shutdown
Shutdown		20	°C	Below the maximum rating of the device being protected
Auto – recoverable	Temperature hysteresis of approximately 10°C provided between shutdown and restart.			

Overcurrent events that exceed the envelope by 5% will hiccup continuously at a frequency of approximately once every 20 seconds. For voltage set – points below 42V, a tracking Under Voltage shutdown occurs at 2 volts below set-point. UV must exhibit for more than 1 second before shutdown. UV shutdown will exhibit the same 20 second hiccup behavior.

Auxiliary Output

Parameter	Min	Typ	Max	Units	Notes
Output Voltage Setpoint		5		V_{DC}	
Output Current	0.005		0.75	A	
Overall Regulation	-10		+5	%	Within ±5% when load is < 0.5A.
Ripple and Noise		50	100	mV_{pk-pk}	20MHz bandwidth
Over – voltage Clamp			7	V_{DC}	
Over – current Limit	110		175	%FL	

Technical Specifications (continued)

Environmental, EMC, Reliability Specifications

Environmental

Parameter	Min	Typ	Max	Units	Notes
Ambient Temperature					
Operating	-40[5]		55	°C	Air inlet from sea level to 5,000 feet.
Derating		1	2	°C	Per 1,000 feet above 5,000 feet.
Storage Temperature	-40		85	°C	
Humidity	5		95	%	Relative humidity, non-condensing
Altitude	-60		4000	m	For operation above 2500m (5000 ft.), maximum operating temperature is derated by 2°C per 305m (1000 ft.).
	-200		13000	ft	
Shock and Vibration					IPC9592 sections 5.2.8 – 5.2.13
Earthquake Rating	4			Zone	Per Telcordia GR-63-CORE, all floors, when installed in CP Shelf.
Acoustic Noise		55		dBA	Noise is proportional to fan speed, load and ambient temperature.
Harmonic Emissions	Per EN/IEC61000-3-2				
Radiated Emissions[6]	Exceeds FCC and CISPR22 (EN55022) – Class A by a 6dB margin				
Conducted Emissions – ac	Exceeds FCC and CISPR22 (EN55022) Class A Telcordia GR-1089-CORE - Class A by a 6dB margin				
ESD	Error free per EN/IEC 61000-4-2 Level 3 (6 kV contact discharge, 8 kV air discharge).				
Radiated Immunity	Error free per EN/IEC 61000-4-3 Level 3 (10 V/m).				
Electrical Fast Transient Burst	Error free per EN/IEC 61000-4-4 Level 3 (2 kV, 5 kHz repetition rate)				
Lightning Surge, Error Free	EN/IEC61000-4-5 Level 4 (4 kV common mode, 2 kV differential mode).				
Damage Free	ANSI C62.41 Level A3 (6 kV common and differential mode)				
Line sags and interruptions	IPC9592A issued May 2010;1 cycle interruption or 25% sag (115V, 230V – nominal for UUT) for 2 seconds the output shall stay above 40V_{DC} at full load. [Note: An input sag below 80V may cause an immediate shutdown].				
Conducted Immunity	Error free per EN/IEC 61000-4-6 Level 3 (10V_{rms}).				
Reliability (calculated)		450,000		Hours	At ambient of 25°C at full load per Telcordia SR-332, issue 2, Reliability Prediction for Electronic Equipment, Method I Case III.
Isolation					
Input – Chassis/Signals	1500			V_{rms}	Per EN60950.
Input – Output	3000			V_{rms}	Consult factory for testing to this requirement
Output – Chassis	500			V_{DC}	Internal Lineage standard, GR_947
Output – Chassis/Signals	2250			V_{DC}	POE compliant Rectifier, Per IEEE802.3.
Service Life		10		Years	25°C ambient, full load excluding fans.

[5]Designed to start and work at an ambient as low as -40°C, but may not meet operational limits until above -5°C

[6]Radiated emissions compliance was met using a Lineage Power shelf. This shelf includes output common and differential mode capacitors that assist in meeting compliance.

Control and Status

The Rectifier provides three means for monitor/ control: analog, PMBus™, or the ABB Galaxy – based RS485 protocol.

Details of analog control and the PMBus™ based protocol are provided in this data sheet. ABB will provide separate application notes on the Galaxy RS485 based protocol for users to interface to the rectifier. Contact your local ABB representative for details.

Signal Reference

Unless otherwise noted, all signals are referenced to Logic_GRD. See the Signal Definitions Table at the end of this document for further description of all the signals.

Logic_GRD is isolated from the main output of the power supply for PMBus communications. Communications and the 5V standby output are not connected to main power return (Vout(-)) and can be tied to the system digital ground point selected by the user. (Note that RS485 communications is referenced to Vout(-), main power return of the power supply).

Logic_GRD is capacitively coupled to Frame_GRD inside the power supply. The maximum voltage differential between Logic_GRD and Frame_GRD should be less than $100V_{DC}$.

Control Signals

Enable: Controls the main $48V_{DC}$ output when either analog control or PMBus protocols are selected, as configured by the Protocol pin. This pin must be pulled low to turn **ON** the rectifier. The rectifier will turn **OFF** if either the **Enable** or the **ON/OFF** pin is released. This signal is referenced to Logic_GRD. In RS485 mode this pin is ignored.

ON/OFF: This is a shorter pin utilized for hot-plug applications to ensure that the rectifier turns **OFF** before the power pins are disengaged. It also ensures that the rectifier turns **ON** only after the power pins have been engaged. Must be connected to V_OUT (-) for the rectifier to be ON.

Margining: The $48V_{DC}$ output can be adjusted between 18 – $58V_{DC}$ by a control voltage on the Margin pin. This control voltage can be generated either from an external voltage source, or by forming a voltage divider between 3.3V and Logic_GRD, as shown in Fig. 1. The power supply includes the high side pull-up 10kΩ resistor to $3.3V_{DC}$. Connecting a resistor between the margin pin and Logic_GRD will complete the divider.

An open circuit, or a voltage level > $3.0V_{DC}$, on this pin sets the main output to the factory default setting of $48V_{DC}$.

Hardware margining is only effective until software commanded output voltage changes are not executed. Software commanded output voltage settings permanently override the hardware margin setting until power to the internal controller is interrupted, for example if input power or bias power is recycled.

The controller always restarts into its default configuration, programmed to set the output as instructed by the margin pin. Subsequent software commanded settings permanently override the margin pin. Adding a resistor between margin and Vout(-) is an ideal way of changing the factory set point of the rectifier to whatever voltage level is desired by the user.

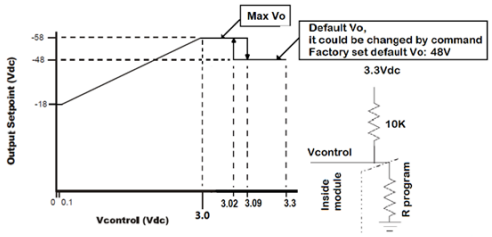


Figure 1. Diagram showing how output can be margined using Vcontrol adjustment.

Module Present Signal: This signal has dual functionality. It can be used to alert the system when a rectifier is inserted. A 500Ω resistor is present in series between this signal and Logic_GRD. An external pull-up should not raise the voltage on the pin above $0.25V_{DC}$. When the voltage on this pin exceeds $1V_{DC}$, the write_protect feature of the EEPROM is enabled.

Technical Specifications (continued)

8V_INT: Single wire connection between modules, Provides bias to the DSP of an unpowered module.

Reset: This is a PCA9541 multiplexer function utilized during PMBus communications. If momentarily grounded (Logic_GRD), the multiplexer would reset itself.

Protocol: Establishes the communications mode of the rectifier, between analog/PMBus and RS485 modes. For RS485, connect a 10kΩ pull-down resistor from this pin to V_OUT(-). For analog/ PMBus leave the pin open. Do not tie this signal pin to V_OUT(-) because that connection configures the internal DSP into a reprogrammed state.

Unit Address: Each module has an internal 10kΩ resistor pulled up between unit_address and 3.3V_{DC}. A resistor between unit_address and Vout(-) sets the appropriate unit address.

			I^2C address	
Rectifier	**Resistor Value**	**Nominal voltage**	**A1**	**A0**
1	30K	2.477	0	0
2	14K	1.925	0	1
3	6K	1.243	1	0
4	2.5K	0.654	1	1

Shelf Address: By applying the required voltage between the shelf address pin and Vout(-), up to 8 different shelves and so up to 32 different modules can be addressed using either the PMBus or ABB Galaxy based RS485 protocol.

PMBus addressing is limited to a maximum of 8 modules and so the software decodes the shelf address setting into either shelf 0 or shelf 1 in PMBus applications. If more than two shelves are paralleled, the user must separate the I^2C lines so that address conflicts do not occur.

Shelf_address	**1**	**2**	**3**	**4**
Maximum voltage	3.45	2.97	2.56	2.14
Nominal voltage	3.30	2.86	2.4	1.96
Minimum voltage	3.00	2.60	2.18	1.73
Address bit – A2	0	1	0	1

Shelf_address	**5**	**6**	**7**	**8**
Maximum voltage	1.70	1.25	0.80	0.25
Nominal voltage	1.50	1.10	0.60	0.01
Minimum voltage	1.29	0.84	0.30	0
Address bit – A2	0	1	0	1

Status Signals

Power Capacity: A HI on this pin indicates that the rectifier delivers high line rated output power; a LO indicates that the rectifier is connected to low line configured for 1200W operation.

Power Fail Warning: This signal is HI when the main output is being delivered and goes LO for the duration listed in this data sheet prior to the output decaying below the listed voltage level.

Fault: This signal goes LO for any failure that requires rectifier replacement. These faults may be due to:

- Fan failure
- Over – temperature warning
- Over – temperature shutdown
- Over – voltage shutdown
- Internal Rectifier Fault

Digital Feature Descriptions

PMBus™ compliance: The power supply is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements with the following exceptions:
The power supply continuously updates its STATUS and ALARM registers to the latest state in order to capture the 'present' state of the power supply. There are a number of indicators, such as those indicating a communications fault (PEC error, data error) that do not get cleared until specifically instructed by the host controller sending a clear_faults command. A 'bit' indicator notifies the user if the STATUS and ALARM registers changed since the last 'read' by the host controller.
For example, if a voltage surge causes a momentary shutdown for over voltage the power supply will automatically restart if the 'auto_restart' feature is invoked. During the momentary shutdown the power supply issues an Alert# indicating to the system controller that a status change has occurred. If the system controller reads back the STATUS and ALARM registers while the power supply is shut down it will get the correct fault condition. However, inquiry of the state of the power supply after the restart event would indicate that the power supply is functioning correctly. The STATUS and ALARM indicators did not freeze at the original shutdown state and so the reason for the original Alert# is erased. The restart 'bit' would be set to indicate that an event has occurred.

The power supply also clears the STATUS and ALARM registers after a successful read back of the information in these registers, with the exception of communications error alarms. This automated process improves communications efficiency since the host controller does not have to issue another clear_faults command to clear these registers.

Dual, redundant buses: Two independent I^2C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the power supply. For example, a short or an open connection in one of the I^2C lines does not affect communications capability on the other I^2C line. Failure of a 'master' controller does not affect the power supplies and the second 'master' can take over control at any time.

Using the PCA9541 multiplexer: Transition between the two I^2C lines is provided by the industry standard PCA9541 I^2C master selector multiplexer. Option 01 of the device code is supplied which, upon start – up, connects channel 0 to the power supply. In this fashion applications using only a single I^2C line can immediately start talking across the bus without first requiring to reconfigure the multiplexer.

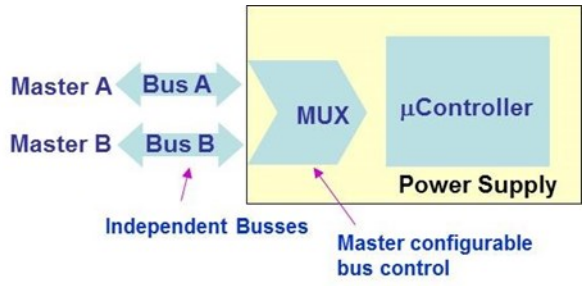


Figure 2: Diagram showing conceptual representation of the dual I^2C bus system.

Control can be taken over at any time by a specific 'master' even during data transmission to the other 'master'. The 'master' needs to be able to handle incomplete transmissions in the multi – master environment in case switching should commence in the middle of data transmission.

Master/Slave: The 'host controller' is always the MASTER. Power supplies are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

Clock stretching: The power supply may initiate clock stretching if it is busy. The 'slave' may keep the clock LO until it is ready to receive instructions. The maximum clock stretch interval is 25ms.

The host needs to refrain from issuing the next clock signal until the clock is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the power supply.

Note that clock stretching occurs after the 9th (ACK) bit, the exception being the START command.

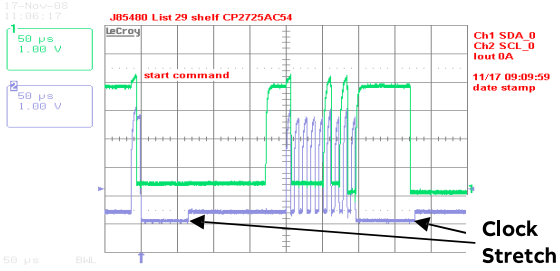


Figure 3: Example waveforms showing clock stretching.

Communications speed: Both 100kHz and 400kHz clock rates are supported. The power supplies default to the 100kHz clock rate.

Packet Error Checking: The power supply will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the correct command is executed.

PEC is a CRC – 8 error – checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

SMBusAlert#: The power supply can issue SMBAlert# driven from either its internal micro controller (µC) or from the PCA9541 I^2C bus master selector. That is, the SMBAlert# signal of the internal µC funnels through the PCA9541 master selector that buffers the SMBAlert# signal and splits the signal to the two SMBAlert# signal pins exiting the power supply. In addition, the PCA9541 signals its own SMBAlert# request to either of the two SMBAlert# signals when required.

Non-supported commands: Non-supported commands are flagged by setting the appropriate STATUS bit and issuing an SMBAlert# to the 'host' controller.

Data out-of-range: The power supply validates data settings and sets the data out-of-range bit and SMBAlert# if the data is not within acceptable range.

SMBAlert# triggered by the µC: The µC driven SMBAlert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the power supply has changed states and the signal will be latched LO until the power supply receives a 'clear' instruction as outlined below. If the alarm state is still present after the 'clear_faults' command has been received, then the signal will revert back into its LO level again and will latch until a subsequent 'clear' signal is received from the host controller.

The signal will be triggered for any state change, including the following conditions;

- V_{IN} under or over voltage
- V_{out} under or over voltage
- I_{OUT} over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- Internal faults

The power supply will clear the SMBusAlert# signal (release the signal to its HI state) upon the following events:

- Completion of a 'read_status' instruction
- Receiving a CLEAR_FAULTS command
- The main output recycled (turned OFF and then ON) via the ENABLE signal pin
- The main output recycled (turned OFF and then ON) by the OPERATION command

SMBAlert# triggered by the PCA9541: If clearing the Alert# signal via the clear_faults or read back fails, then reading back the Alert# status of the PCA9541 will be necessary followed by clearing of the PCA9541 Alert#.

The PCA9541 can issue an Alert# even when single bus operation is selected where the bus master selector has not been used or addressed. This may occur because the default state of the PCA9541/01 integrated circuit issues Alert# to both I^2C lines for all possible transitioning states of the device. For example, a RESET caused by a glitch would cause the Alert# to be active.

If the PCA9541 is not going to be used in a specific application (such as when only a single I^2C line is utilized), it is imperative that interrupts from the PCA9541 are de - activated by the host controller. To de-activate the interrupt registers the PCA9541 the 'master' needs to address the PCA9541 in the 'write' mode, the interrupt enable (IE) register needs to be accessed and the interrupt masks have to be set to HI '1'. (Note: do not mask bit 0 which transmits Alert# from the power supply). This command setting the interrupt enable register of the PCA9541 is shown below;

Start	Unit Address								ACK
1	7	6	5	4	3	2	1	0	1
S	1	1	1	0	A2	A1	A0	0	A

Command Code	ACK	IE Register	Stop
8	1	8	
0x00	A	0x0E	P

There are two independent interrupt enable (IE) registers, one for each controller channel (I^2C-0 and I^2C-1). The interrupt register of each channel needs to be configured independently. That is, channel I^2C-0 cannot configure the IE register of I^2C-1 or viseversa.

This command has to be initiated to the PC9541 only once after application of power to the device. However, every time a restart occurs the PCA9541 has to be reconfigured since its default state is to issue Alert# for changes to its internal status.

If the application did not configure the interrupt enable register the Alert# line can be cleared (de – activated), if it has been activated by the PCA9541, by reading back the data from the interrupt status registers (Istat).

Refer to the PCA9541 data sheet for further information on how to communicate to the PCA9541 multiplexer.

Please note that the PCA9541 does not support Packet Error Checking (PEC).

Re-initialization: The I^2C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I^2C µController does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, It had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few µseconds required to accomplish re-initialization the I^2C µController may not recognize a command sent to it. (i.e. a start condition).

Global broadcast: This is a powerful command because it can instruct all power supplies to respond simultaneously in one command. But it does have a serious disadvantage. Only a single power supply needs to pull down the ninth acknowledge bit. To be certain that each power supply responded to the global instruction, a READ instruction should be executed to each power supply to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Note: The PCA9541 I^2C master selector does not respond to the GLOBAL BROADCAST command.

Read back delay: The power supply issues the SMBAlert # notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive SMBAlert# could be triggered by the transitioning state of the power supply. In order to avoid successive SMBAlert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an SMBAlert# before executing a read back. This delay will ensure that only the final state of the power supply is captured.

Successive read backs: Successive read backs to the power supply should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

Device ID: Address bits A2, A1, A0 set the specific address of the power supply. The least significant bit x (LSB) of the address byte configures write [0] or read [1] events. In a **write** command the system instructs the power supply. In a **read** command information is being accessed from the power supply.

	Address Bit							
	7	6	5	4	3	2	1	0
PCA9541	1	1	1	0	A2	A1	A0	R/W
Micro controller	1	0	0	0	A2	A1	A0	R/W
External EEPROM	1	0	1	0	A2	A1	A0	R/W
Global Broadcast	0	0	0	0	0	0	0	0
	MSB							LSB

The **Global Broadcast** instruction executes a simultaneous **write** instruction to all power supplies. A **read** instruction cannot be accessed globally. The three programmable address bits are the same for all I^2C accessible devices within the power supply.

Technical Specifications (continued)

PMBus™ Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

Master to Slave Slave to Master

SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read, A – Acknowledge, NA – not-acknowledged, P – Stop

Direct mode data format: The Direct Mode data format is supported, where $y = [mX + b] \times 10^{R}$. In the equation, y is the data value from the controller and x is the 'real' value either being set or returned, except for V_{IN} and Fan speed, x is the data value from the controller and y is the 'real' value.

For example, to set the output voltage to $50.45V_{DC}$, Multiply the desired set point by the m constant, 50.45 x 400 = 20,180. Convert this binary number to its hex equivalent: 20,180b = 0x4ED4. The result is sent LSB=0xD4 first, then MSB=0x4E.

The constants are

Function	Operation	m	b	R
Output voltage Output voltage shutdown	Write / read	400	0	0
Output Current	read	5	0	0
Temperature	read	1	0	0
Input Voltage	read	1	75	0
Input Power	read	1	0	0
Fan Speed setting (%)	read	1	0	0
Fan speed in RPM	read	100	0	0

PMBus™ Command set:

Command	Hex Code	Data Field	Function
Operation	01	1	Output ON/OFF
Clear_Faults	03	0	Clear Status
Vout_command	21	2	Set Vout
Vout_OV_fault_limit	40	2	Set OV fault limit
Read_status	D0	10	Read Status, Vout, Iout, T
LEDs test ON	D2	0	Test LEDs
LEDs test OFF	D3	0	
Enable_write	D6	0	Enable EEPROM write
Disable_write	D7	0	Disable EEPROM write
Inhibit_restart	D8	0	Latch upon failure
Auto_restart	D9	0	Hiccup
Isolation_test	DA	0	Perform isolation test
Read_input_string	DC	2	Read Vin and Pin
Read_firmware_rev	DD	3	Firmware revisions
Read_run_timer	DE	3	Accumulated ON state
Fan_speed_set	DF	3	Fan speed control
Fan_normal_speed	E0	0	Stop fan control
Read_fan_speed	E1	4	Fan control & speed
Stretch_LO_25ms	E2	0	Production test feature

Command Descriptions

Operation (01h): By default the Power supply is turned **ON** at power up as long as REMOTE ON is active LO. The Operation command is used to turn the Power Supply ON or OFF via the PMBus. The data byte below follows the OPERATION command.

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

To **RESET** the power supply cycle the power supply OFF, wait at least 2 seconds, and then turn back ON. All alarms and shutdowns are cleared during a restart.

Clear_faults (03h): This command clears information bits in the STATUS registers, these include:

- Isolation OK
- Isolation test failed
- Restarted OK
- Invalid command
- Invalid data
- PEC error

Vout_Command (21h) : This command is used to change the output voltage of the power supply. Changing the output voltage should be performed simultaneously to all power supplies operating in parallel using the Global Address (Broadcast) feature.

If only a single power supply is instructed to change its output, it may aattempt to source all the required power which can cause either a power limit or shutdown condition.

Software programming of output voltage overrides the set point voltage configured during power_up. The program no longer looks at the 'margin pin' and will not respond to any hardware voltage setting. The default state cannot be accessed any longer unless power is removed from the DSP.

To properly hot-plug a power supply into a live backplane, the system generated voltage should get re-configured into either the factory adjusted firmware level or the voltage level reconfigured by the margin pin. Otherwise, the voltage state of the plugged in power supply could be significantly different than the powered system.

Voltage margin range: $42V_{DC} – 58V_{DC}$.

A voltage programming example: The task: set the output voltage to $50.45V_{DC}$

The constants for voltage programming are: m=400, b and R=0. Multiply the desired set point by the m constant, 50.45x400=20,180. Convert this binary number to its hex equivalent: 20,180b=4ED4h. Transmit the data LSB first, followed by MSB, 0 x D44Eh.

Vout_OV_fault_limit (40h) : This command sets the Output Overvoltage Shutdown level.

Manufacturer-Specific PMBus™ Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the power supply. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No – ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Read_status (D0h) : This 'manufacturer specific' command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = 9	A

8	1	8	1	8	1
Status – 2	A	Status – 1	A	Alarm – 2	A

8	1	8	1	8	1
Alarm – 1	A	Voltage LSB	A	Voltage MSB	A

8	1	8	1	8	1	1
Current	A	Temperature	A	PEC	NA	P

Status and alarm registers

The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are accessed rapidly, at once, using the 'multi parameter' read back scheme of this document. There are a total of four registers. All errors, 0 – normal, 1 – alarm.

Status – 2

Bit	Title	Description
7	PEC Error	Mismatch between computed and transmitted PEC. The instruction has not been executed. Clear_Flags resets this register.
6	Will Restart	Restart after a shutdown = 1
5	Invalid Instruction	The instruction is not supported. An ALERT# will be issued. Clear_Flags resets this register.
4	Power Capacity	High line power capacity = 1
3	Isolation test failed	Information only to system controller
2	Restarted ok	Informs HOST that a successful RESTART occurred clearing the status and alarm registers
1	Data out of range	Flag appears until the data value is within range. A clear_flags command does not reset this register until the data is within normal range.
0	Enable pin HI	State of the ENABLE pin, HI = 1 = OFF

Isolation test failed: The 'system controller' has to determine that sufficient capacity exists in the system to take a power supply 'off line' in order to test its isolation capability. Since the power supply cannot determine whether sufficient redundancy is available, the results of this test are provided, but the 'internal fault' flag is not set.

Status – 1

Bit	Title	Description
7	spare	
6	Isolation test OK	Isolation test completed successfully.
5	Internal fault	The power supply is faulty
4	Shutdown	
3	Service LED ON	ON = 1
2	External fault	the power supply is functioning OK
1	LEDs flashing	LEDs tested test ON = 1
0	Output ON	ON = 1

Alarm – 2

Bit	Title	Description
7	Fan Fault	
6	No primary	No primary detected
5	Primary OT	Primary section OT
4	DC/DC OT	DC/DC section OT
3	Output voltage lower than bus	Internal regulation failure
2	Thermal sensor failed	Internal failure of a temperature sensing circuit
1	5V out_of_limits	Either OVP or OCP occurred
0	Power Delivery	A power delivery fault occurred

Power Delivery: The power supply compares its internal sourced current to the current requested by the current share pin. If the difference is > 10A, a fault is issued.

Alarm – 1

Bit	Title	Description
7	Unit in power limit	An overload condition that results in constant power
6	Primary fault	Indicates either primary failure or INPUT not present. Used in conjunction with bit – 0 and Status_1 bits 2 and 5 to assess the fault.
5	Over temp. shutdown	One of the over_temperature sensors tripped the supply
4	Over temp warning	Temperature is too high, close to shutdown
3	In over current	Shutdown is triggered by low output voltage < $39V_{DC}$.
2	Over voltage shutdown	
1	V_{out} out_of_limits	Indication the output is not within design limits. This condition may or may not cause an output shutdown.
0	V_{in} out_of_limits	The input voltage is outside design limits

LEDS test ON (D2h) : Will turn – ON simultaneously the two front panel LEDs of the Power supply sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the power supply being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

LEDS test OFF (D3h) : Will turn – OFF simultaneously the two front panel LEDs of the Power supply.

Service LED ON (D4h) : Requests the power supply to **flash** – ON the Service (ok-to-remove) LED. The **flash** sequence is approximately 0.5 seconds ON and 0.5 seconds OFF.

Service LED OFF (D5h) : Requests the power supply to turn OFF the Service (ok-to-remove) LED.

Enable write (D6h) : This command enables write permissions into the upper ¼ of memory locations for the external EEPROM. A write into these locations is normally disabled until commanded through I^2C to permit writing into the protected area. A delay of about 10ms is required from the time the instruction is requested to the time that the power supply actually completes the instruction.

See the FRU – ID section for further information of content written into the EEPROM at the factory.

Disable write (D7h) : This command disables write permissions into the upper ¼ of memory locations for the external EEPROM.

Unit in Power Limit or in Current Limit: When output voltage is > $36V_{DC}$ the Output LED will continue blinking.

When output voltage is < $36V_{DC}$, if the unit is in the RESTART mode, it goes into a hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF. When the unit is in latched shutdown the output LED is OFF.

Inhibit_restart (D8h) : The **Inhibit – restart** command directs the power supply to remain latched off for over_voltage, over_temperature and over_current. The command needs to be sent to the power supply only once. The power supply will remember the INHIBIT instruction as long as internal bias is active.

Restart after a lachoff: To restart after a latch_off either of four restart mechanisms are available. The hardware pin **Enable** may be turned OFF and then ON. The unit may be commanded to restart via I^2C through the Operation command by first turning OFF then turning ON. The third way to restart is to remove and reinsert the unit. The fourth way is to turn OFF and then turn ON ac power to the unit.

The fifth way is by changing firmware from **latch off** to **restart.** Each of these commands must keep the power supply in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the **Status_2** register.

A power system that is comprised of a number of power supplies could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual power supplies. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all power supplies.
2. Toggling Off and then ON the REMOTE ON signal.
3. Removing and reapplying input commercial power to the entire system.

The power supplies should be turned OFF for at least 20-30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual power supplies.

Auto_restart (D9h) : Auto – restart is the default configuration for overvoltage, overcurrent and overtemperature shutdowns.

However, overvoltage has a unique limitation. An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

This command resets the power supply into the default auto-restart configuration.

Isolation test (DAh): This command verifies functioning of output OR'ing. At least two paralleled power supplies are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test can fail. Only one power supply should be tested at a time.

Verifying test completion should be delayed for approximately 30 seconds to allow the power supply sufficient time to properly execute the test.

Failure of the isolation test is not considered a power supply FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

Read input string (DCh) : Reads back the input voltage and input power consumed by the power supply. In order to improve the resolution of the input voltage reading the data is shifted by 75V.

1	7	1	1	8
S	Slave address	Wr	A	Command Code 0xDC

1	1	7	1	1
A	Sr	Slave Address	Rd	A

8	1	8	1
Byte Count = 4	A	Voltage	A

8	1	8	1	8	1	1
Power – LSB	A	Power – MSB	A	PEC	No – ack	P

Read_firmware_rev [0 x DD]: Reads back the firmware revision of all three µC in the power supply.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDD	A

1	1	7	1	1	8	1
A	Sr	Slave Address	Rd	A	Byte Count = 4	A

8	1	8	1
Primary micro revision	A	DSP revision	A

8	1	8	1	1
I^2C Micro revision	A	PEC	No – ack	P

For example; the read returns one byte for each device (i.e. 0 x 002114h). The sequence is primary micro, DSP, and I^2C micro. 0x00 in the first byte indicates that revision information for the primary micro is not supported. The number 21 for the DSP indicates revision 2.1, and the number 14 for the I^2C micro indicates revision 1.4.

Read_run_timer [0 x DE]: This command reads back the recorded operational ON state of the power supply in hours. The operational ON state is accumulated from the time the power supply is initially programmed at the factory. The power supply is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is approximately 10 years.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code 0xDE	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	Byte count = 4	A

8	1	8	1	8	1
Time – LSB	A	Time	A	Time – MSB	A

8	1	1
PEC	No – ack	P

Fan_speed_set (DFh) : This command instructs the power supply to increase the speed of the fan. The transmitted data byte represents the hex equivalent of the duty cycle in percentage, i.e. 100% = 0 x 64h. The command can only increase fan speed, it cannot instruct the power supply to reduce the fan speed below what the power supply requires for internal control.

Fan_normal_speed (E0h): This command returns fan control to the power supply. It does not require a trailing data byte.

Read_Fan_speed (E1h) : Returns the commanded fan speed in percent and the measured fan speed in RPM from the individual fans. Up to 3 fans are supported. If a fan does not exist (units may contain from 1 to 3 fans), or if the command is not supported the unit return 0x00.

1	8	1	8	1
S	Slave address Wr	A	Command 0xE1	A

1	8	1	8	1
Sr	Slave address Rd	A	Byte count = 5	A

8	1	8	1	8	1	8	1
Adjustment %	A	Fan – 1	A	Fan – 2	A	Fan – 3	A

8	1	1
PEC	NA	P

Stretch_LO_25ms (E2h) : Command used for production test of the clock stretch feature.

None supported commands or invalid data: The power supply notifies the MASTER if a non-supported command has been sent or invalid data has been received. Notification is implemented by setting the appropriate STATUS and ALARM registers and setting the SMBAlert# flag.

Fault Management

The power supply records faults in the STATUS and ALARM registers above and notifies the MASTER controller as described in the **Alarm Notification** section of the non-conforming event.

The STATUS and ALARM registers are continuously updated with the latest event registered by the rectifier monitoring circuits. A host responding to an SMBusALERT# signal may receive a different state of the rectifier if the state has changed from the time the SMBusALERT# has been triggered by the rectifier.

The power supply differentiates between **internal faults** that are within the power supply and **external faults** that the power supply protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or I^2C alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed by looking at the input LEDs. These fault categorizations are predictive in nature and therefore there is a likelihood that a categorization may not have been made correctly.

Input voltage out of range: The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

State Change Definition

A **state_change** is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a **state_change**;

- Initial power – up of the system when AC gets turned ON .This is the indication from the rectifier that it has been turned ON. Note that the master needs to read the status of each power supply to reset the system_interrupt. If the power supply is back-biased through the 8V_INT or the 5VSTB it will not issue an SMBALERT# when AC power is turned back ON.
- Whenever the power supply gets hot-plugged into a working system. This is the indicator to the system (MASTER) that a new power supply is on line.
- Any changes in the bit patterns of the STATUS and ALARM registers are a STATUS change which triggers the SMBALERT# flag. Note that a host-issued command such as CLEAR_FAULTS will not trigger an SMB.

Hot plug procedures

Careful system control is recommended when hot plugging a power supply into a live system. It takes about 15 seconds for a power supply to configure its address on the bus based on the analog voltage levels present on the backplane. If communications are not stopped during this interval, multiple power supplies may respond to specific instructions because the address of the hot plugged power supply always defaults to xxxx000 (depending on which device is being addressed within the power supply) until the power supply configures its address.

The recommended procedure for hot plug is the following: The system controller should be told which power supply is to be removed. The controller turns the service LED ON, thus informing the installer that the identified power supply can be removed from the system. The system controller should then poll the module_present signal to verify when the power supply is re-inserted. It should time out for 15 seconds after this signal is verified. At the end of the time out all communications can resume.

Predictive Failures

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the power supply. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the power supply is not warranted.

Another example of potential predictive failure mechanisms can be derived from information such as fan speed when multiple fans are used in the same power supply. If the speed of the fans varies by more than 20% from each other, this is an indication of an impending fan wear out.

The goal is to identify problems early before a protective shutdown would occur that would take the power supply out of service.

External EEPROM

A 64k-bit EEPROM is provided across the I^2C bus. This EEPROM is used for both storing FRU_ID information and for providing a scratchpad memory function for customer use.

Functionally the EEPROM is equivalent to the ST M34D64 part that has its memory partitioned into a write protected upper ¼ of memory space and the lower ¾ section that cannot be protected. FRU_ID is written into the write protected portion of memory.

Write protect feature: Writing into the upper ¼ of memory can be accomplished either by hardware or software.

The power supply pulls down the write_protect (Wp) pin to ground via a 500Ω resistor between the 'module_present' signal pin and Logic_GRD (see the Module Present Signal section of Input Signals). Writing into the upper ¼ of memory can be accomplished by pulling HI the module_present pin.

An alternative, and the recommended approach, is to issue the Enable_write command via software.

Page implementation: The external EEPROM is partitioned into 32 byte pages. For a write operation only the starting address is required. The device automatically increments the memory address for each byte of additional data it receives. However, if the 32 byte limit is exceeded the device executes a wrap – around that will start rewriting from the first address specified. Thus byte 33 will replace the first byte written, byte 34 the second byte and so on. One needs to be careful therefore not to exceed the 32 byte page limitation of the device.

Table 1: FRU_ID

The upper quarter of memory starting from address 6144 shall be reserved for factory ID and factory data.

Memory Location Decimal	Memory Location (HEX)	Length (bytes)	Format	Static Value type	Description	Notes/Example
6144d	0x1800	12	ASCII	Fixed	ABB – energy – Product ID	CP2725AC54TE
6156d	0x180C	10	ASCII	Fixed	ABB – energy – Part Number	123456789x or C123456789
6166d	0x1816	6	ASCII	Variable	ABB – energy – Hardware revision	x:xxxx controlled by PDI series #
6172d	0x181C	6	ASCII	Variable	spare	
6178d	0x1822	14	ASCII	Variable	ABB – energy – Serial_No	01KZ51018193xx 01 …. Year of manufacture – 2001 KZ … factory, in this case Matamoros 51 .. week of manufacture 018193xx serial # mfg choice
6192d	0x1830	40	ASCII	Variable	ABB – Manufacturing location	"Matamoros, Tamps, Mexico"
6232d	0x1858	8	ASCII	Fixed	spare	
6240d	0x1860	2	HEX	Fixed	spare	
6242d	0x1862	158	ASCII	Fixed	Customer Information	These fields are reserved for use by the customer.
6400d	0x1900	5	HEX	Fixed	M, B, & R for voltage read	M & B are 2 bytes each sent as MSB and then LSB. R is one byte. These are stored as two's complement. See the section on Direct Mode Constants Stored in the EEPROM for the constants stored in these fields
6405d	0x1905	5	HEX	Fixed	M, B, & R for current read	
6410d	0x190A	5	HEX	Fixed	M, B, & R temp read	
6415d	0x190F	5	HEX	Fixed	spare	
6420d	0x1914	5	HEX	Fixed	M, B, & R for voltage set	
6425d	0x1919	5	HEX	Fixed	M, B, & R for input voltage read	
6430d	0x191E	1	HEX	Variable	Validation CHKSUM	
6431d	9x191F	5	HEX	Fixed	M, B, & R for input power read	
6436d	0x1924	5	HEX	Fixed	M, B, & R for fan percent adjust	
6441d	0x1929	5	HEX	Fixed	M, B, & R for fan RPM read	
6446d	0x192E	5	HEX	Fixed	M, B, & R for converter input voltage read	

Notes: Memory locations 0x00 to 0x17FF and 0x1A00 to 0x2000 are blank (0xFF). Locations 0x1800 to 0x19FF contain FRUID, locations not specified are filled with 0's. Checksum is the complement of the sum of locations 0x1800 to 0x19FF (chksum = 0xFF – sum(0x1800 – 0x19FF)), excluding serial number field (checksum will always be the same since all fields are fixed except serial number).

Table 2: Alarm and LED state summary

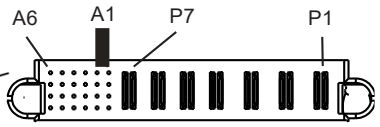
Condition	Power Supply LED State				Monitoring Signals			
	AC OK Green	DC OK Green	Service Amber	Fault Red	Fault	OTW	PFW	Module Present
OK	1	1	0	0	HI	HI	HI	LO
Thermal Alarm (5C before shutdown)	1	1	1	0	HI	LO	HI	LO
Thermal Shutdown	1	0	1	1	LO	LO	LO	LO
Defective Fan	1	0	0	1	LO	HI	LO	LO
Blown AC Fuse in Unit	1	0	0	1	LO	HI	LO	LO
AC Present but not within limits	Blinks	0	0	0	HI	HI	—[4]	LO
AC not present[1]	0	0	0	0	HI	HI	LO	LO
Boost Stage Failure	1	0	0	1	LO	HI	LO	LO
Over Voltage Latched Shutdown	1	0	0	1	LO	HI	LO	LO
Over Current	1	Blinks	0	0	HI	HI	LO	LO
Non – catastrophic Internal Failure[2]	1	1	0	1	LO	HI	HI	LO
Missing Module								HI
Standby (remote)	1	0	0	0	HI	HI	LO	LO
Service Request (PMBus mode)	1	1	Blinks	0	HI	HI	HI	LO
Communications Fault (RS485 mode)	1	1	0	Blinks	HI	HI	HI	LO

[1]This signal is correct if the rectifier is back biased from other rectifiers in the shelf .
[2]Any detectable fault condition that does not cause a shutting down. For example, ORing FET failure, boost section out of regulation, etc.
[3]Signal transition from HI to LO is output load dependent
[4]The PFW signal changes states when the boost voltage decays and not when the AC is out of regulation.

Technical Specifications (continued)

Output Connector

Mating Connector: right angle PWB mate – all pins: AMP 1450572 – 1, right angle PWB mate except pass – thru input power: AMP 6450378-1



Manufacturer part numbers: FCI 51939-568

	SIGNAL						OUTPUT POWER				INPUT POWER		
	6	5	4	3	2	1	P7	P6	P5	P4	P3	P2	P1
A	SCL_0	MOD_PRES	PFW	LOGIC_GRD	RS_485+	UNIT_ADDR							
B	SCL_1	OTW	Alert#_0	Alert#_1	RS_485-	8V_INT	V_OUT	V_OUT	V_OUT	V_OUT	EARTH	LINE-2	LINE-1
C	SDA_0	Margin	Enable	Reset	Ishare	Protocol	(-)	(+)	(+)	(-)	(GND)	(Neutral)	(HOT)
D	SDA_1	Fault	5VA	Power_Cap	ON/OFF	SHELF_ADDR							

Note: Connector is viewed from the rear positioned inside the rectifier
Signal pins columns 1 and 2 are referenced to V_OUT (-)
Signal pins columns 3 through 6 are referenced to Logic GRD
Last to make-first to break shortest pin
Earth — First make-last to break longest pin implemented in the mating connector

Signal Definitions

All hardware alarm signals (Fault, PFW, OTW, Power Capacity) are open drain FETs. These signals should be pulled HI to either 3.3V or 5V. Maximum sink current 5mA. An active LO signal (< 0.4V_{DC}) state. All signals are referenced to Logic GRD unless otherwise stated. Contact your Lineage Power representative for more details.

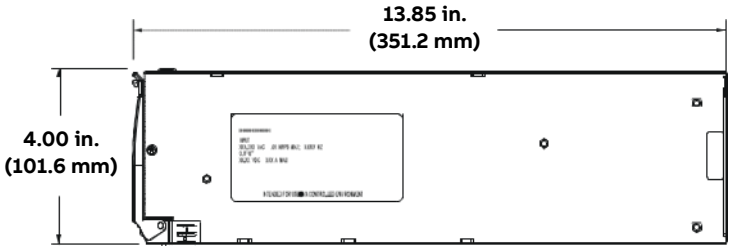
Function	Label	Type	Description
Output Enable	Enable	Input	If shorted to LOGIC_GRD, the Rectifier output is enabled when using I^2C mode of operation. May also be toggled to reset a latched OFF Rectifier. Function not available in RS485 mode.
Power Fail Warning	PFW	Output	An open drain FET; normally HI, indicating output power is present. Changes to LO at least 5msec before the output voltage decays below 40V_{DC}.
I^2C Interrupt	Alert#_0 Alert#_1	Output	Interrupt signal via I^2C lines indicating that service is requested from the host controller. This signal pin is pulled up to 3.3V via a 10kΩ resistor and switches to active LO when an interrupt occurs.
Rectifier Fault	Fault	Output	Indicates that an internal fault exists. An open drain FET; normally HI, changes to LO.
Module Present	MOD_PRES	Output	Short pin, see Status and Control description for further information on this signal.
ON/OFF	ON/OFF	Input	Short pin, connects last and breaks first; used to activate and deactivate output during hot – insertion and extraction, respectively. Ref: Vout (-)
Protocol select	Protocol	Input	See Status and Control description for further information on this signal. Ref: Vout(-).
Margining	Margin	Input	Allows changing of output voltage through an analog voltage input or via resistor divider.
Over – Temperature Warning	OTW	Output	An open drain FET; normally HI, changes to LO approximately 5°C prior to thermal shutdown.
Power Capacity	POWER_CAP	Output	Open drain FET; Used to indicate Rectifier operation mode; HI indicates 2250W operation and LO indicates 1200W operation.
Rectifier address	Unit_addr	Input	Voltage level addressing of Rectifiers within a single shelf. Ref: Vout (-).
Shelf Address	Shelf_addr	Input	Voltage level addressing of Rectifiers within multiple shelves. Ref: Vout (-).
Back bias	8V_INT	Bi-direct	Diode OR'ed 8V_{DC} drain; used to back bias microprocessors and DSP of failed Rectifier from operating Rectifiers. Ref: Vout (-).
Mux Reset	Reset	Input	Resets the I^2C lines to I^2C line 0.
Standby power	5VA	Output	5V at 0.75A provided for external use by either adjacent power supplies or the using system.
Current Share	Ishare	Bi – direct	A single wire interface between each of the power unit forces them to share the load current. Ref: Vout (-).
I^2C Line 0	SCL_0, SDA_0	Input	I^2C line 0.
I^2C Line 1	SCL_1, SDA_1	Input	I^2C line 1.
I^2C Interrupt	Alert#_0, Alert#_1	Output	Goes active LO
RS485 Line	RS_485+ RS_485-	Bi – direct	RS485 line.

Technical Specifications (continued)

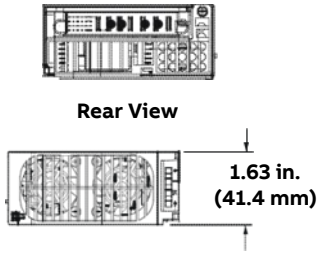
Front Panel LEDs

	Analog Mode	I²C Mode	RS485 Mode
☐ ~	←	**ON:** Input ok **Blinking:** Input out of limits	→
☐ =	←	**ON:** Output ok **Blinking:** Overload	→
☐ 🛠	**ON:** Over – temperature Warning	**ON:** Over – temperature Warning **Blinking:** Service	**ON:** Over – temperature Warning
☐ !	←	**ON:** Fault	→ **ON:** Fault **Blinking:** Not communicating

Dimensions



Top View



Faceplate color shall be dark grey with a green hinge

Physical

Packaged weight	5.4/2.45 lbs/kgs
Unpacked weight	4.8/2.18 lbs/kgs
Heat release	100 Watts or 341 BTUs @ 80% load, 153 Watts or 522 BTUs @ 100% load

Ordering Information

Item	Description	Ordering Code
CP2000AC48TEZ – FB2	$52V_{DC}$ @ 43.3A, $5V_{DC}$ @ 0.75A, RoHS Complaint, conformal coated	1600158237A

Change History (excludes grammar & clarifications)

Revision	Date	Description of Changes
1.0	02/09/2023	Initial release

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