<Full SiC Power Modules>

FMF800DXZ-24B

HIGH POWER SWITCHING USE
INSULATED TYPE

Dual switch (Half-Bridge)

Drain current I_D .... **800** A

Drain-Source voltage V_{DSX} .... **1200** V

Maximum junction temperature T_{vjmax} .... **175** °C

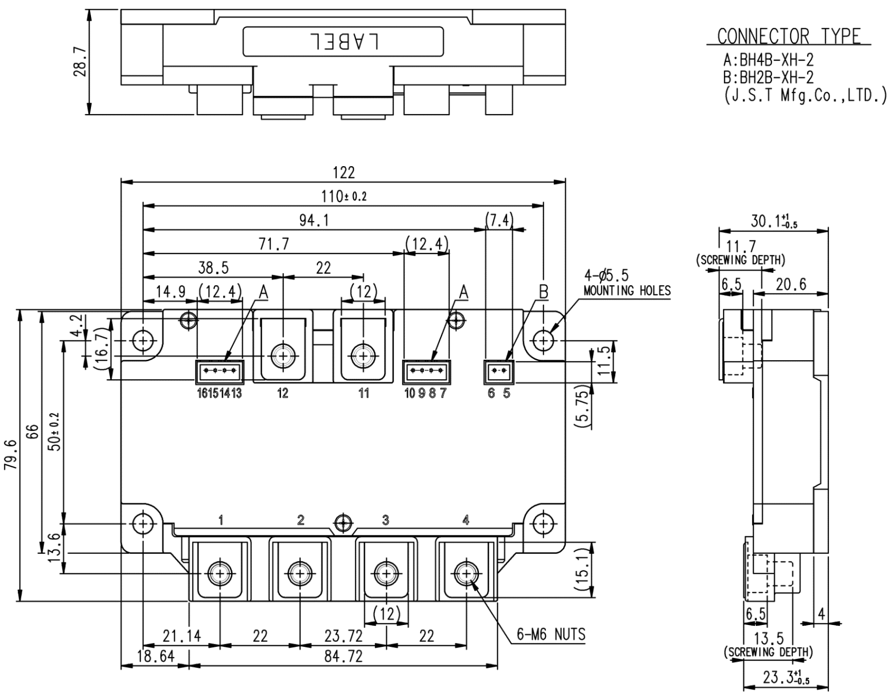
- Silicon Carbide MOSFET + Silicon Carbide Schottky Barrier Diode
- Flat base Type
- Copper base plate
- RoHS Directive compliant
- Recognized under UL1557, File E323585

APPLICATION

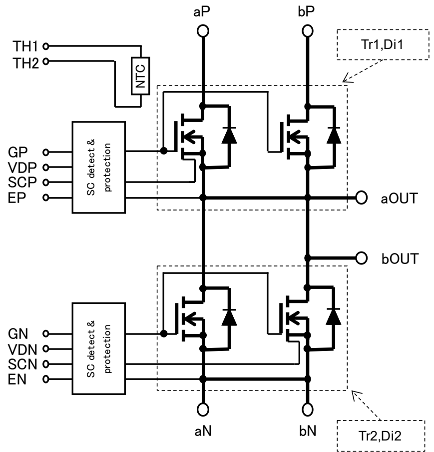
AC Motor Control, Motion/Servo Control, Power supply, etc.

OUTLINE DRAWING & INTERNAL CONNECTION

Dimension in mm



INTERNAL CONNECTION



Terminal	code
1	aP
2	aN
3	bN
4	bP
5	TH1
6	TH2
7	VDN
8	SCN
9	GN
10	EN
11	bOUT
12	aOUT
13	EP
14	GP
15	SCP
16	VDP

Tolerance otherwise specified

Division of Dimension	Tolerance
0.5 to 3	±0.2
over 3 to 6	±0.3
over 6 to 30	±0.5
over 30 to 120	±0.8
over 120 to 400	±1.2

aP and bP, aN and bN, aOUT-bOUT must be connected externally.

MAXIMUM RATINGS (T_{vj} =25 °C, unless otherwise specified)

Symbol	Item	Conditions	Rating	Unit
V_{DSX}	Drain-source voltage	V_{GS}=-15 V	1200	V
V_{GSS}	Gate-source voltage	D-S short-circuited	±20	V
I_D	Drain current	DC, T_C=60℃ (Note.2)	800	A
I_{DRM}	Drain current	Pulse, Repetitive (Note.3), T_{vj}=150℃ (Note.4)	1200	A
P_{tot}	Total power dissipation	T_C=25 °C (Note. 2)	3120	W
I_S (Note.1)	Source current	DC	800	A
I_{SRM} (Note.1)	Source current	Pulse, Repetitive (Note.3), T_{vj}=150℃	1200	A
V_{isol}	Isolation voltage	Terminals to base plate, RMS, f=60 Hz, AC 1 min	5000	V
T_{vjmax}	Maximum junction temperature	Instantaneous event (overload) (Note.10)	175	°C
T_{vjop}	Operating junction temperature	Continuous oepration (under switching) (Note.10)	-40～+150	°C
T_{cmax}	Maximum case temperature	(Note.2, 10)	125	°C
T_{stg}	Storage temperature	-	-40～+125	°C

ELECTRICAL CHARACTERISTICS (T_{vj}=25 °C, unless otherwise specified)

Symbol	Item	Conditions (note9)		Limits Min.	Limits Typ.	Limits Max.	Unit
I_{DSX}	Drain-source cut-off current	V_{DS}=V_{DSX}, V_{GS}=-15 V		-	-	8	mA
		V_{DS}=800V, V_{GS}=-15 V		-	-	0.8	mA
$V_{GS(th)}$	Gate-source threshold voltage	I_D=228 mA, V_{DS}=10 V		1.8	2.5	3.2	V
I_{GSS}	Gate-source leakage current	V_{GS}=V_{GSS}, D-S short-circuited		-	-	0.5	μA
$V_{DS(on)}$ (terminal)	Drain-source on-state voltage	I_D=800 A, V_{GS}=15V (Note.6)	T_{vj}=25 °C	-	1.65	2.30	V
			T_{vj}=125 °C	-	2.10	-	V
			T_{vj}=150 °C	-	2.20	-	V
$V_{DS(on)}$ (chip)	Drain-source on-state voltage	I_D=800 A, V_{GS}=15V (Note.6)	T_{vj}=25 °C	-	1.35	-	V
			T_{vj}=125 °C	-	1.80	-	V
			T_{vj}=150 °C	-	1.90	-	V
$r_{DS(on)}$ (chip)	Drain-source on-state resistance	I_D=800 A, V_{GS}=15V (Note.6)	T_{vj}=25 °C	-	1.7	-	mΩ
			T_{vj}=125 °C	-	2.3	-	mΩ
			T_{vj}=150 °C	-	2.4	-	mΩ
C_{iss}	Input capacitance	V_{DS}=10 V, V_{GS}=0V		-	68	-	nF
C_{oss}	Output capacitance	V_{DS}=10 V, V_{GS}=0V		-	49	-	nF
C_{rss}	Reverse transfer capacitance	V_{DS}=10 V, V_{GS}=0V		-	3.4	-	nF
Q_G	Gate charge	V_{DD}=600 V, I_D=800 A, V_{GS}=0→15 V		-	1950	-	nC
$t_{d(on)}$	Turn-on delay time	V_{DD}=600 V, I_D=800 A, V_{GS}=±15 V, T_{vj}=150℃, R_G=1.5Ω, L_{s_ext}=16nH, Inductive load, per pulse		-	180	-	ns
t_r	Rise time			-	80	-	ns
$t_{d(off)}$	Turn-off delay time			-	450	-	ns
t_f	Fall time			-	50	-	ns
E_{on}	Turn-on switching energy			-	22	-	mJ
E_{off}	Turn-off switching energy			-	33	-	mJ
Q_C	Drain-source charge			-	4	-	μC
V_{SD} (Note.1) (terminal)	Source-drain voltage	I_S=800 A (Note.6) V_{GS}=-15 V	T_{vj}=25 °C	-	1.90	2.45	V
			T_{vj}=125 °C	-	2.70	-	V
			T_{vj}=150 °C	-	2.90	-	V
V_{SD} (Note.1) (chip)	Source-drain voltage	I_S=800 A (Note.6) V_{GS}=-15 V	T_{vj}=25 °C	-	1.60	-	V
			T_{vj}=125 °C	-	2.40	-	V
			T_{vj}=150 °C	-	2.60	-	V
$R_{DD'+SS'}$	Internal lead resistance	P-N, T_C=25℃ (Note.2)		-	0.375	-	mΩ
L_s	Internal stray inductance	P-N		-	10	-	nH
$r_{g(on)}$	Internal gate resistance (on)	Per switch		-	1.04	-	Ω
$r_{g(off)}$	Internal gate resistance (off)	Per switch		-	5.88	-	Ω

THERMAL RESISTANCE CHARACTERISTICS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Thermal resistance (Note. 2)	Junction to case, per inverter switch	-	-	48	K/kW
$R_{th(j-c)D}$		Junction to case, per inverter FWD	-	-	63	
$R_{th(c-s)}$	Contact thermal resistance (Note.2)	Case to heat sink, per 1 module, Thermal grease applied (Note.8, 10)	-	12	-	K/kW

NTC THERMISTOR PART

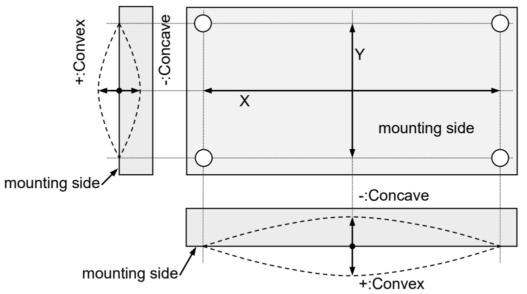
Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
R_{25}	Zero-power resistance	T_C=25 °C (Note.2)	4.85	5.00	5.15	kΩ
ΔR/R	Deviation of resistance	T_C=100 °C (Note.2) ,R_{100}=493 Ω	-7.3	-	+7.8	%
$B_{(25/50)}$	B-constant	Approximate by equation (Note.7)	-	3375	-	K
P_{25}	Power dissipation	T_C=25 °C (Note.2)	-	-	10	mW

MECHANICAL CHARACTERISTICS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
M_t	Mounting torque	Main terminals M 6 screw	3.5	4.0	4.5	N·m
M_s		Mounting to heat sink M 5 screw	2.5	3.0	6.0	
m	mass	-	-	500	-	g
d_a	Clearance		10	-	-	mm
d_s	Creepage distance		17	-	-	mm
e_c	Flatness of base plate	On the centerline X, Y (Note.5)	-100	-	+100	μm
	Connector insertion force	2 pin type	0	-	25	N
		4 pin type	0	-	35	N

*: This product is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU and (EU)2015/863.

Note1. Represent ratings and characteristics of the anti-parallel, source-drain free wheeling diode (FWD).
2. Case temperature (T_C) and heat sink temperature (T_s) are defined on the each surface (mounting side) of base plate and heat sink just under the chips.
Refer to the figure of chip location.
3. Pulse width and repetition rate should be such that the device junction temperature (T_{vj}) does not exceed T_{vjmax} rating.
4. Junction temperature (T_{vj}) should not increase beyond T_{vjmax} rating.
5. The base plate (mounting side) flatness measurement points (X, Y) are as follows of the following figure.



6. Pulse width and repetition rate should be such as to cause negligible temperature rise.
7. $B_{(25/50)} = \ln(\frac{R_{25}}{R_{50}})/(\frac{1}{T_{25}} - \frac{1}{T_{50}})$
R_{25}: resistance at absolute temperature T_{25} [K]; T_{25}=25 [°C]+273.15=298.15 [K]
R_{50}: resistance at absolute temperature T_{50} [K]; T_{50}=50 [°C]+273.15=323.15 [K]
8. Typical value is measured by using thermally conductive grease of λ=0.9 W/(m·K)/$D_{(C-S)}$=100μm.
9. Per switch (ex. Tr1 chips total in page.6)
10. Long term performance related to thermal conductive grease (including but not limited to aspects such as the increase of thermal resistance due to pumping out, etc.) should be verified under your specific application conditions. Each temperature condition ($T_{vj\,max}$, $T_{vj\,op}$, $T_{C\,max}$) must be maintained below the maximum rated temperature throughout consideration of the temperature rise even for long term usage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	(DC) Supply voltage	Applied across aP -aN/ bP-bN terminals	-	600	850	V
V_D	DC supply voltage (control)	Applied across VDP-EP/ VDN-EN terminals	13.5	15.0	16.5	V
$V_{GS(+)}$	Gate-Source positive drive voltage	Applied across GP-EP/ GN-EN terminals	13.5	15.0	16.5	V
$V_{GS(-)}$	Gate-Source negative drive voltage	Applied across GP-EP/ GN-EN terminals	-16.5	-15.0	-7.0	V
R_G	External gate resistance (Note.11)	Per switch	1.5	-	7.5	Ω
f_c	Switching frequency	V_{GS}=±15V, R_G=1.5Ω, V_{DD}=600V, T_{vj}=150℃	-	-	50	kHz
$t_{d(SCoff)}$	Gate cutoff delay time after SC output	V_{GS}=15V, R_G=1.5Ω, V_{DD}=600V, T_{vj}=150℃	-	-	3	μs

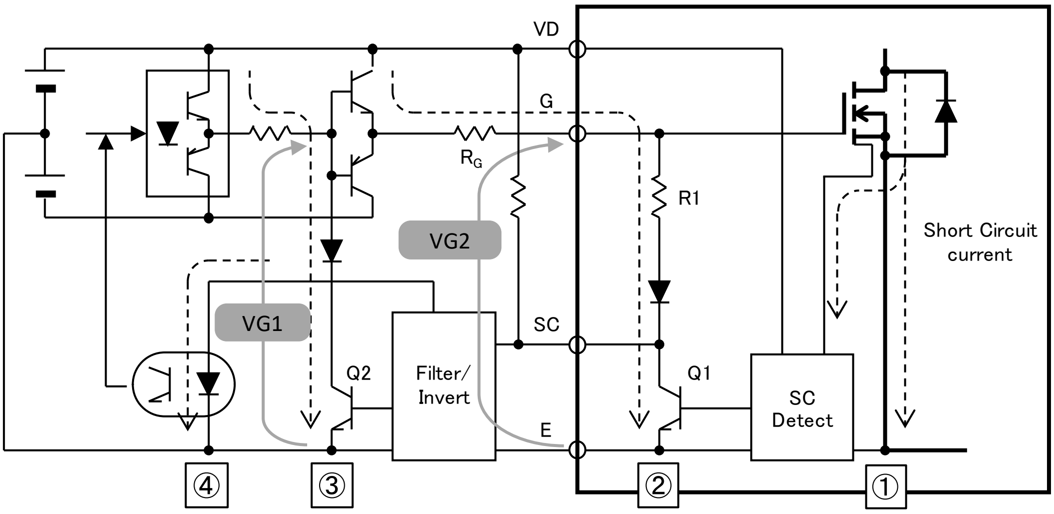
Note 11. The value of external gate resistance should be considered the surge voltage not to exceed the rating voltage in the worst system condition.

SHORT CIRCUIT DETECTION & PROTECTION CHARACTERISTICS

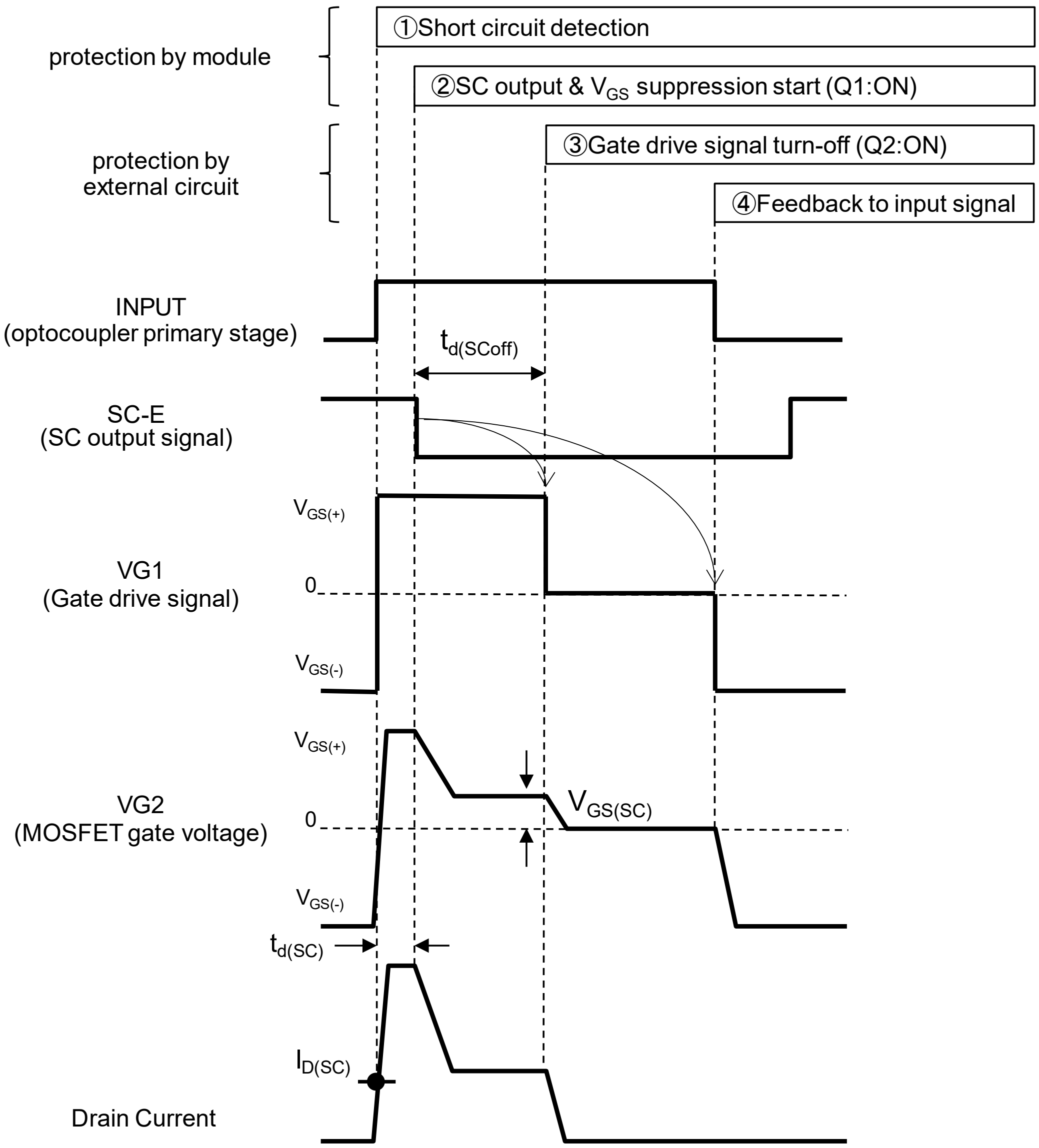
Symbol	Item	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$I_{D(SC)}$	SC detect drain current	T_{vj}=150℃, V_{GS}=15V	1200	1600	-	A
$t_{d(SC)}$	SC detect delay time	T_{vj}=150℃, V_{GS}=15V, R_G=1.5Ω	-	1	-	μs
$V_{GS(SC)}$	SC protection gate limit voltage	T_{vj}=150℃, V_{GS}=15V, R_G=1.5Ω	-	10	-	V
R1	SC protection gate limit resistance	-	-	2.35	-	Ω

Refer to the circuit in page.5

SHORT CIRCUIT DETECTION & PROTECTION



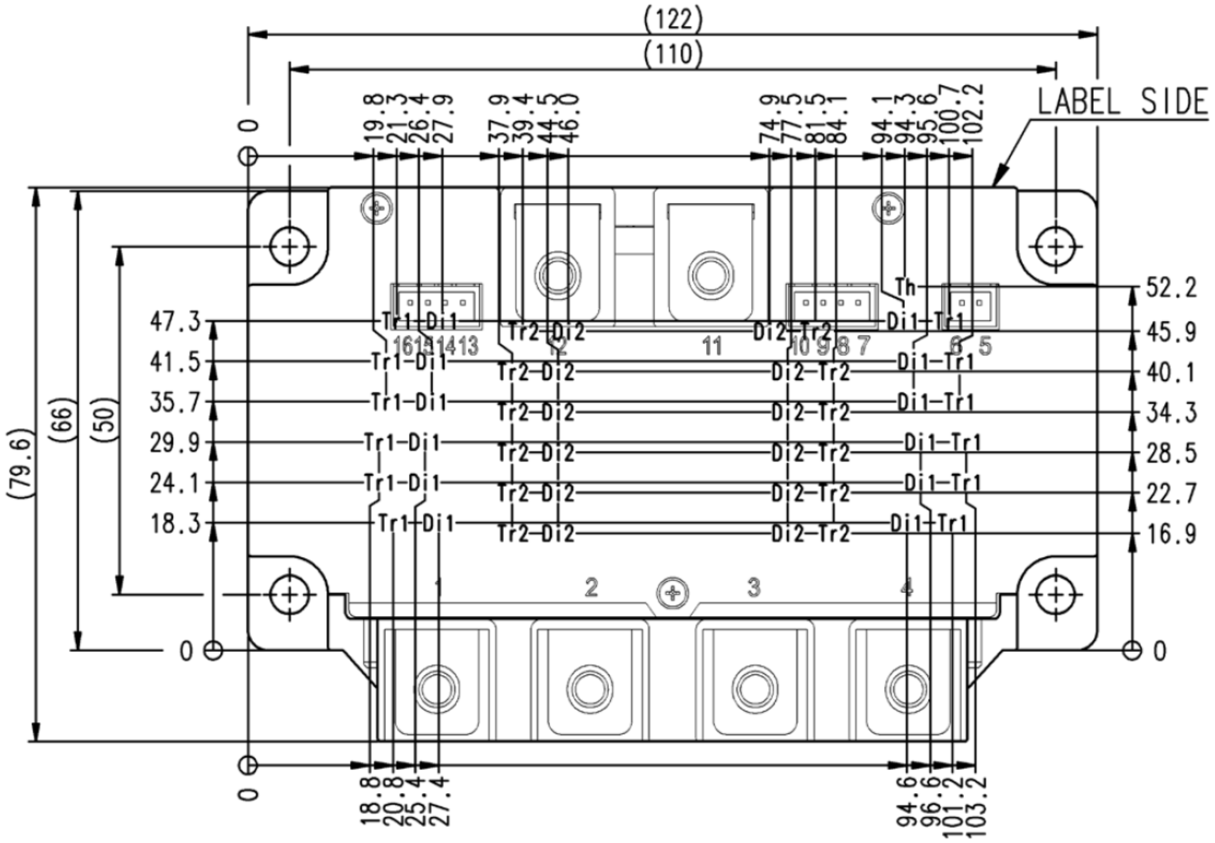
Example of application (Short circuit detection & protection)



Short circuit detection & protection diagram

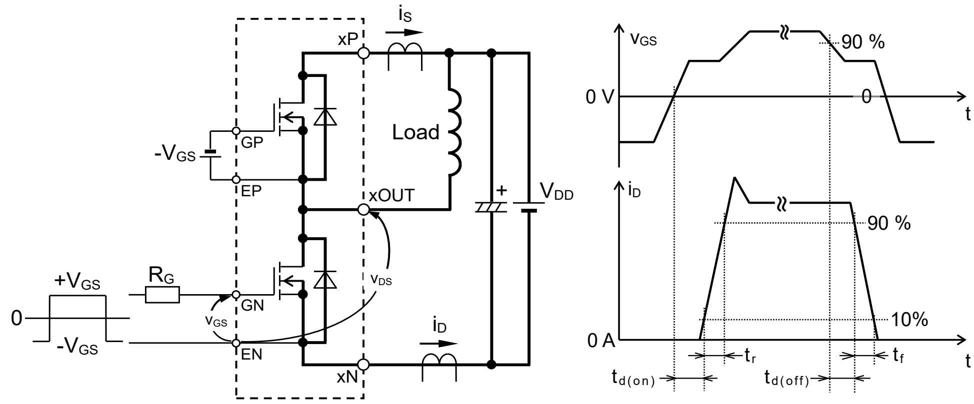
CHIP LOCATION (Top view)

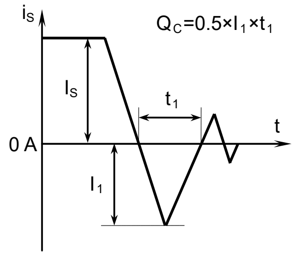
Dimension in mm, tolerance: ±1 mm



Tr1,Tr2: SiC-MOSFET, Di1,Di2: SiC-SBD, Th: NTC thermistor

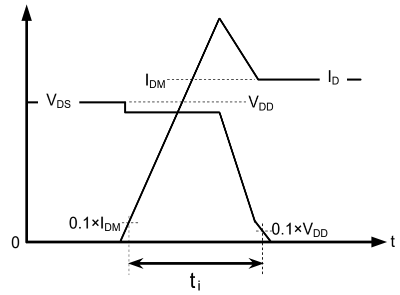
TEST CIRCUIT AND WAVEFORMS



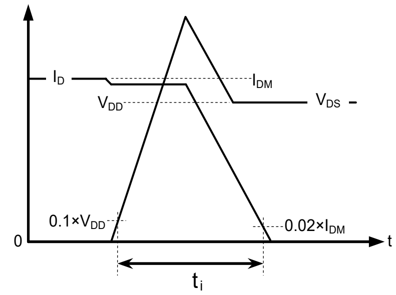


Switching characteristics test circuit and waveforms(x: connected a* and b*)

Q_C test waveform



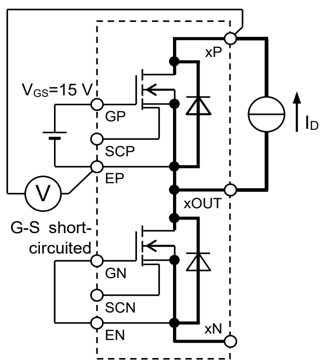
MOSFET Turn-on switching energy



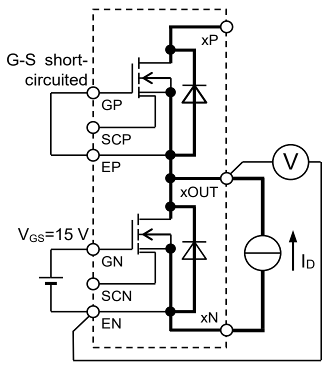
MOSFET Turn-off switching energy

Turn-on / Turn-off switching energy test waveforms (Integral time instruction drawing)

TEST CIRCUIT

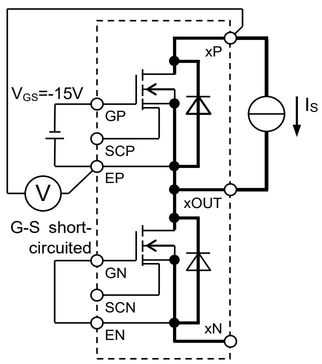


Tr1

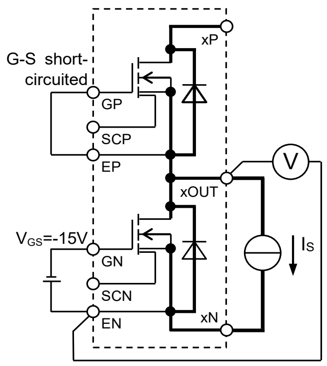


Tr2

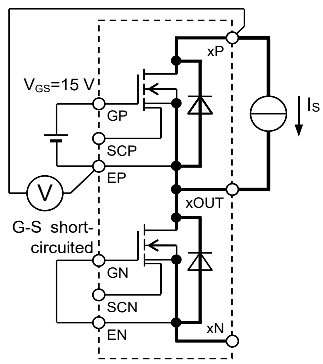
$V_{DS(on)}$ test circuit (x: Connected a* and b*)



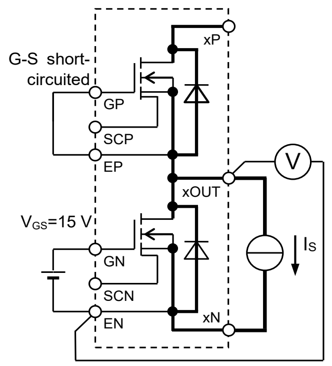
Di1



Di2



Tr1&Di1



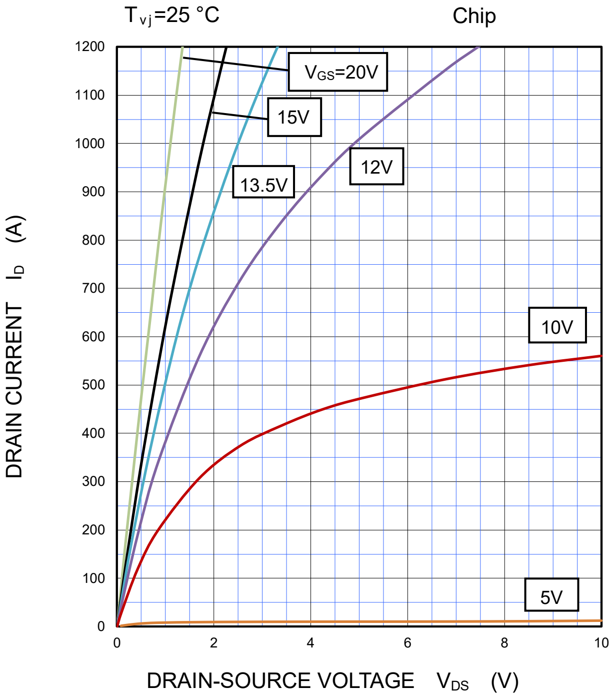
Tr2&Di2

V_{SD} test circuit, V_{GS}=-15V (x: Connected a* and b*)

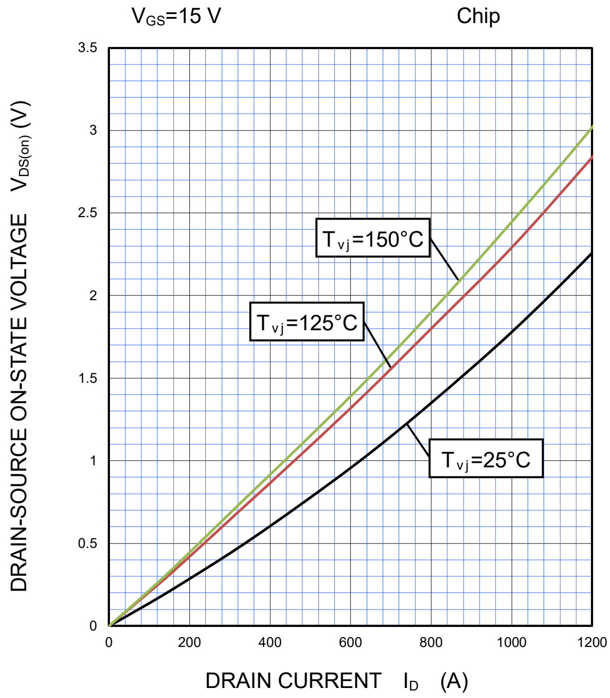
V_{SD} test circuit, V_{GS}=15V (x: Connected a* and b*)

PERFORMANCE CURVES

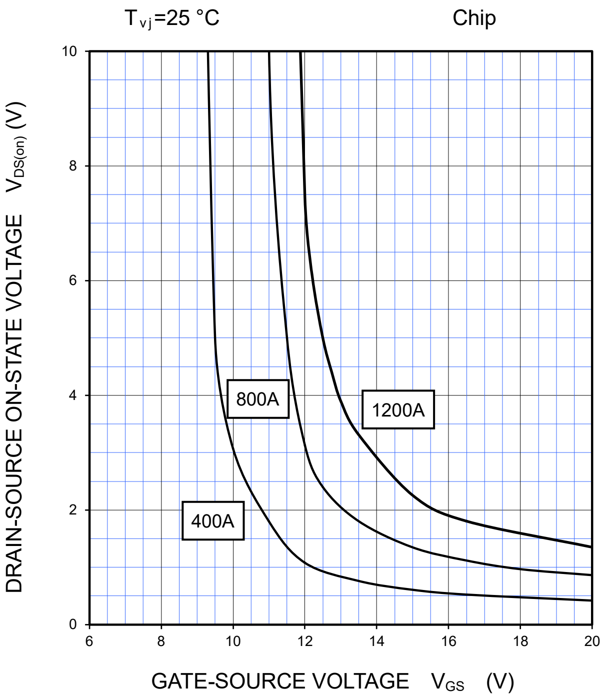
OUTPUT
CHARACTERISTICS
(TYPICAL)



DRAIN-SOURCE ON STATE VOLTAGE
CHARACTERISTICS
(TYPICAL)

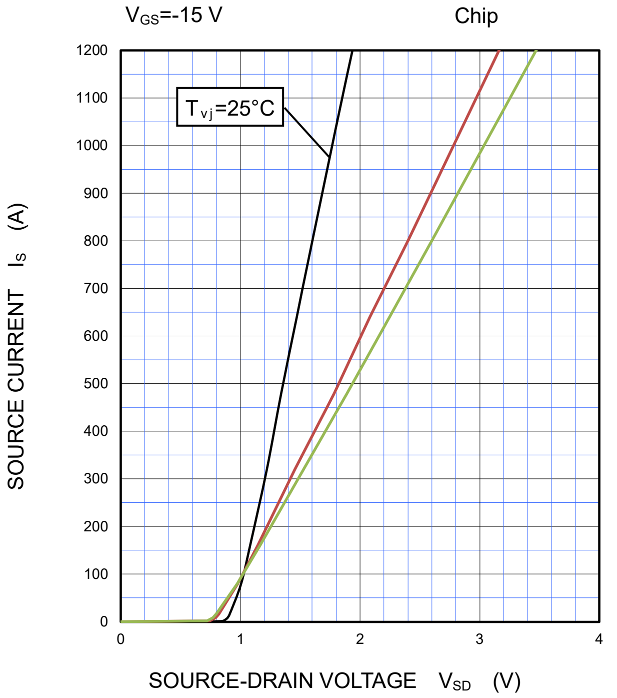


DRAIN-SOURCE ON STATE VOLTAGE
CHARACTERISTICS
(TYPICAL)

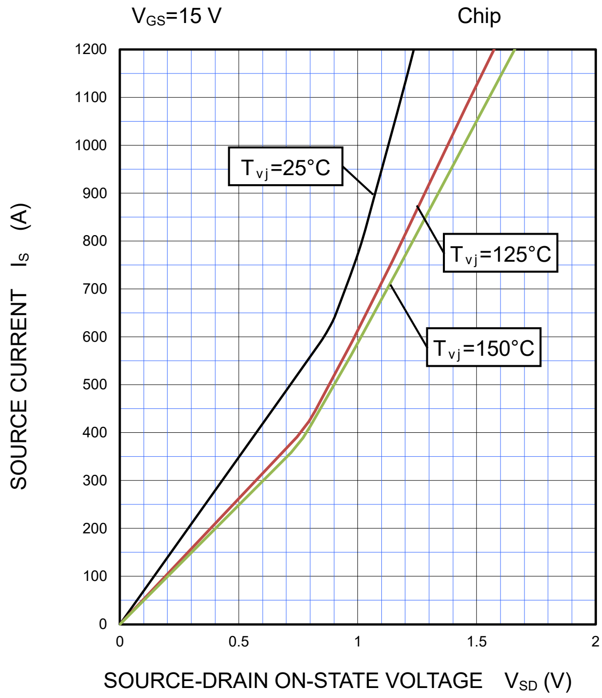


PERFORMANCE CURVES

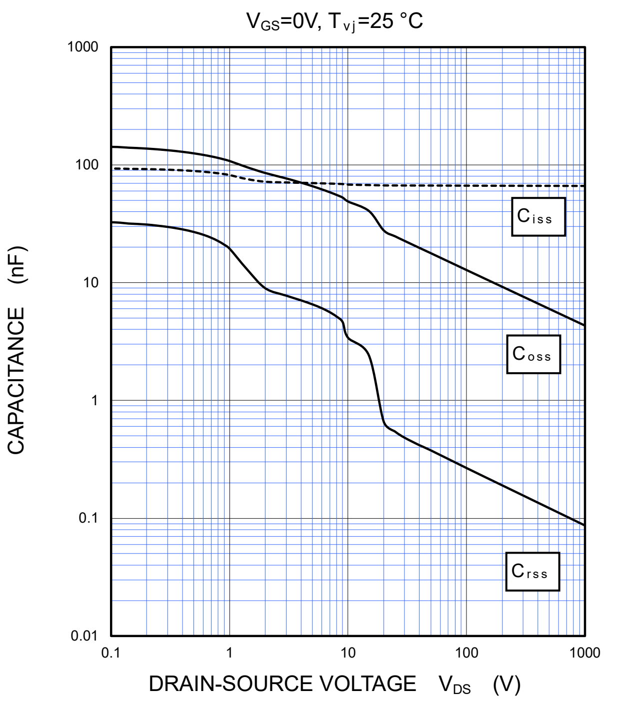
FREE WHEELING DIODE
FORWARD CHARACTERISTICS
(TYPICAL)



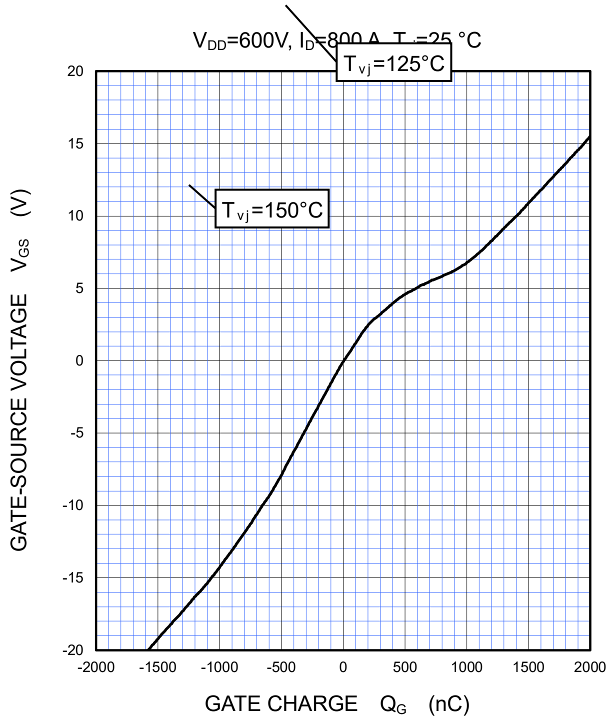
SOURCE-DRAIN ON STATE VOLTAGE
CHARACTERISTICS
(TYPICAL)



CAPACITANCE
CHARACTERISTICS
(TYPICAL)



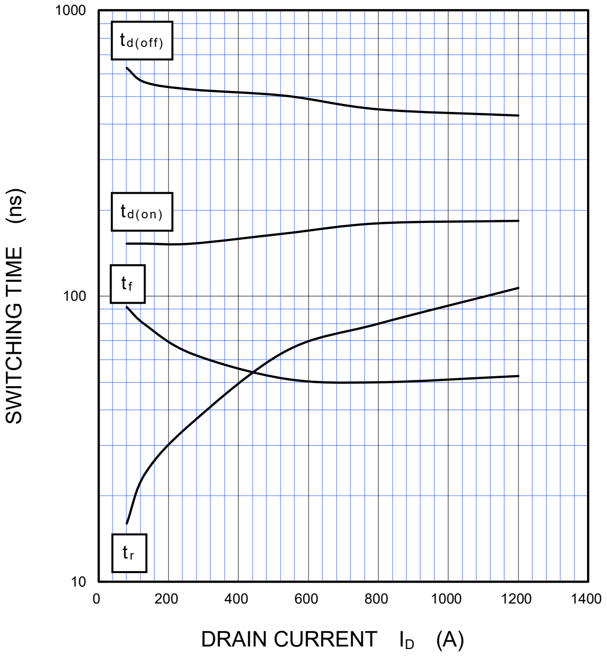
GATE CHARGE
CHARACTERISTICS
(TYPICAL)



PERFORMANCE CURVES

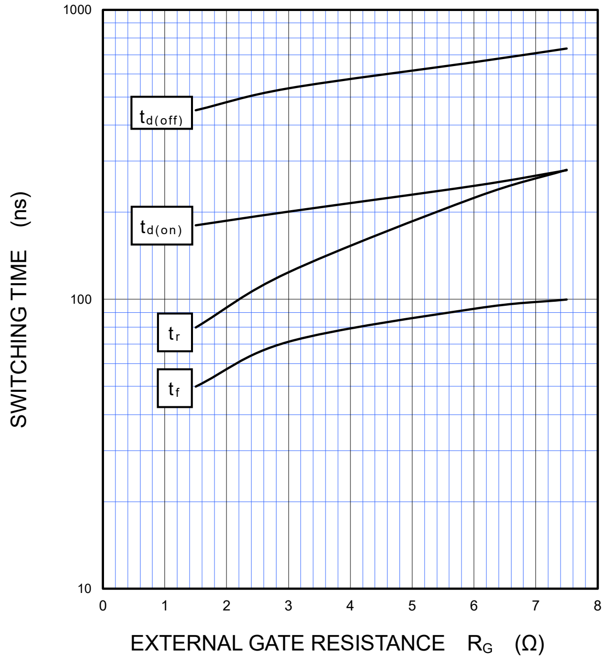
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{DD}=600 V, V_{GS}=±15 V, R_G=1.5 Ω, L_{s_ext}=16nH
T_{vj}=150 °C, INDUCTIVE LOAD



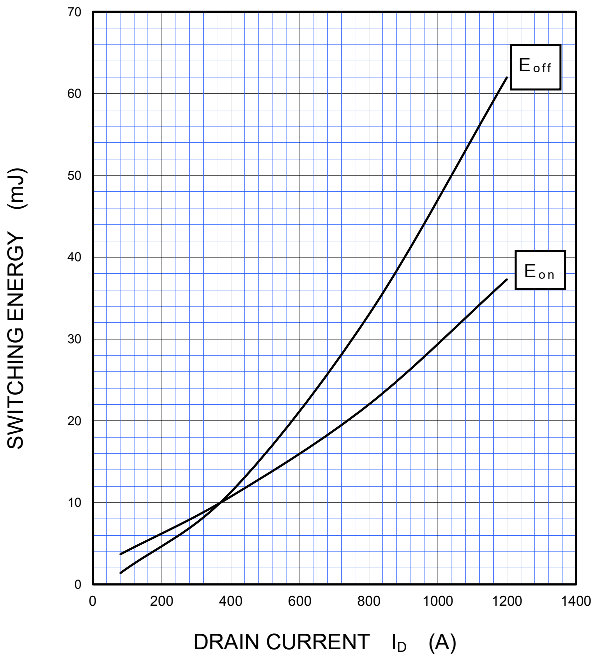
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{DD}=600 V, V_{GS}=±15 V, I_D=800 A, L_{s_ext}=16nH
T_{vj}=150 °C, INDUCTIVE LOAD



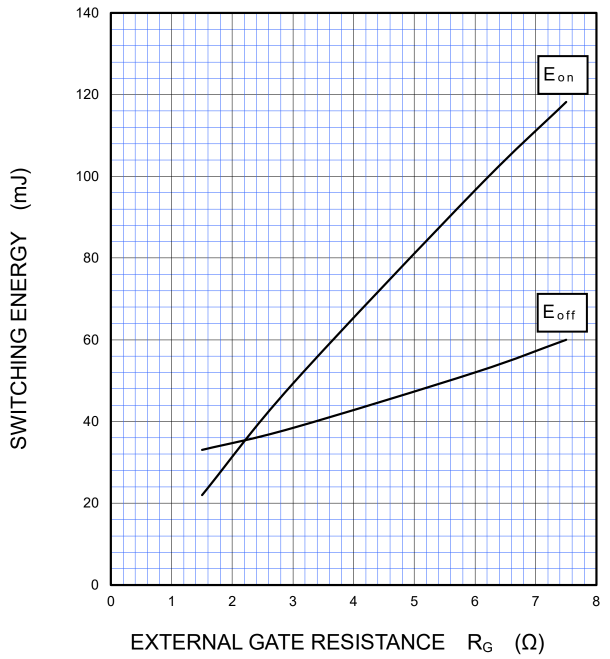
HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

V_{DD}=600 V, V_{GS}=±15 V, R_G=1.5Ω, T_{vj}=150 °C, L_{s_ext}=16nH
INDUCTIVE LOAD, PER PULSE



HALF-BRIDGE
SWITCHING CHARACTERISTICS
(TYPICAL)

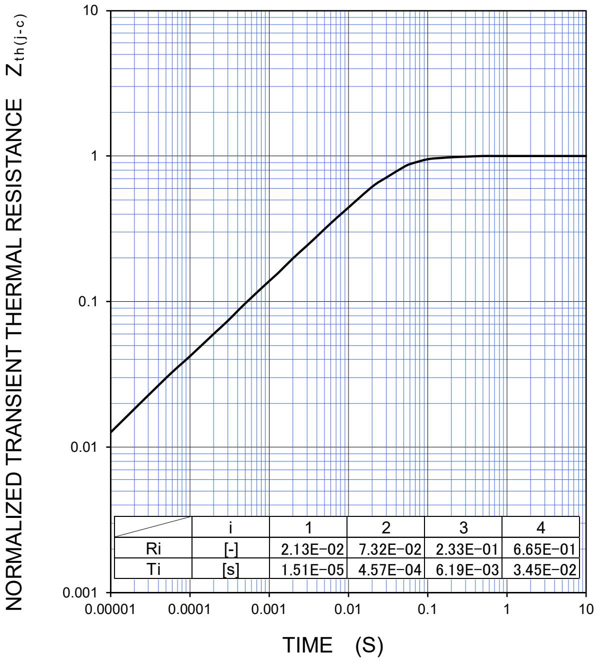
V_{DD}=600 V, V_{GS}=±15 V, I_D=800 A, T_{vj}=150 °C, L_{s_ext}=16nH
INDUCTIVE LOAD, PER PULSE



PERFORMANCE CURVES

TRANSIENT THERMAL IMPEDANCE
CHARACTERISTICS
(MAXIMUM)

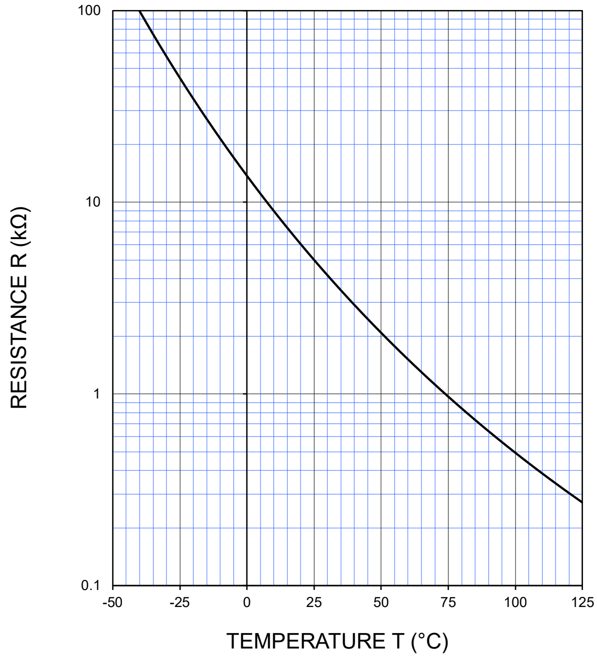
Single pulse, T_C=25 °C
$R_{th(j-c)Q}$=48K/kW, $R_{th(j-c)D}$=63K/kW



	i	1	2	3	4
Ri	[-]	2.13E−02	7.32E−02	2.33E−01	6.65E−01
Ti	[s]	1.51E−05	4.57E−04	6.19E−03	3.45E−02

NTC thermistor part

TEMPERATURE
CHARACTERISTICS
(TYPICAL)



Note: The characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Important Notice

The information contained in this datasheet shall in no event be regarded as a guarantee of conditions or characteristics. This product has to be used within its specified maximum ratings, and is subject to customer's compliance with any applicable legal requirement, norms and standards.
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In usage of power semiconductor, there is always the possibility that trouble may occur with them by the reliability lifetime such as Power Cycle, Thermal Cycle or others, or when used under special circumstances (e.g. condensation, high humidity, dusty, salty, highlands, environment with lots of organic matter / corrosive gas / explosive gas, or situations which terminals of semiconductor products receive strong mechanical stress). Therefore, please pay sufficient attention to such circumstances. Further, depending on the technical requirements, our semiconductor products may contain environmental regulation substances, etc. If there is necessity of detailed confirmation, please contact our nearest sales branch or distributor.

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Keep safety first in your circuit designs!

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