CHT-OPAL DATASHEET

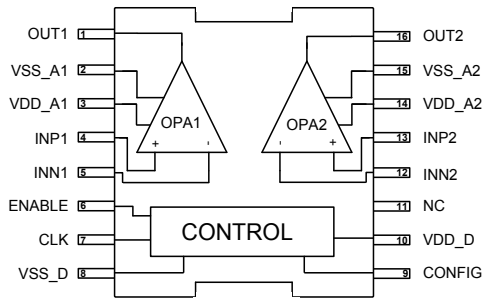
Version: 1.10

High-Temperature, Ultra High-Precision Dual Operational Amplifier

General description

CHT-OPAL is an ultra high-precision, dual operational amplifier designed for applications that require very low offset and very low noise. Both amplifiers can be configured as a differential amplifier or as an instrumentation amplifier (combined with a third, external amplifier cell and with external resistors). Key features include single 5V nominal power supply and rail-to-rail inputs and outputs. Best-in-class precision on the full temperature range -55°C to +225°C encompass low input offset (internally compensated) and low noise. The internal circuitry uses a clock that is internally generated. There is a spread-spectrum mode for this clock. The user can decide not to use this internal clock and rather provide it from external circuitry (e.g. for synchronization purposes).

CHT-OPAL also features a Stand-by mode that disables the two Op Amps and place the circuit in a low power consumption mode when the function is not needed.



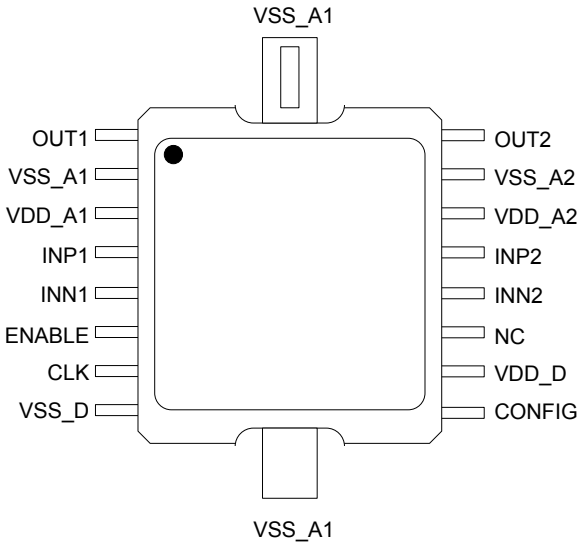
Features

- Junction operating temperature from -55°C to 225°C
- Single supply operation: 5V ±10%
- Low offset: 50µV typ, 100 µV max
- Low noise: 5 µVpp typ
- High CMRR: 85 dB min
- Product gain bandwidth: 2.8 MHz typ
- Slew rate: 2.7 V/µs typ
- Rail-2-rail input and output
- Low bias input current: <10 pA typ
- Quiescent current: 1.2 mA typ.
- Automatic offset compensation
- Stand-by current: 7 µA max
- Latch-up free
- For lower bias input current applications, contact CISSOID
- Package: TDFP16
- Validated at 225°C for 30000 hours (and still on-going)

Applications

- High temperature instrumentation & data acquisition
- Signal conditioning & instrumentation amplifiers for temperature, pressure, motion, speed and position sensors
- Strain gage amplifiers
- Photodiode and PMT amplifiers
- Charge amplifiers
- Current sensing
- Transmitters (4-20mA, etc.)

Pinout



Pin #	Pin Name	Pin Description
1	OUT1	Output OPA1
2	VSS_A1	Negative power supply Analog OPA1
3	VDD_A1	Positive power supply Analog OPA1
4	INP1	Positive input pin OPA1
5	INN1	Negative input pin OPA1
6	ENABLE	Enable input pin[1]
7	CLK	Input clock signal[1]
8	VSS_D	Negative power supply digital part
9	CONFIG	Configuration input pin[1]
10	VDD_D	Positive power supply digital part
11	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
12	INN2	Negative input pin OPA2
13	INP2	Positive input pin OPA2
14	VDD_A2	Positive power supply Analog OPA2
15	VSS_A2	Negative power supply Analog OPA2
16	OUT2	Output OPA2

The 2 vertical large leads are internally connected to VSS_A1 and are also connected to the package heat sink.

[1] Cfr “Mode of operations” for details about function of pins “CLK”, “CONFIG” and “ENABLE”

Absolute Maximum Ratings

$V_{DD\_X} – V_{SS\_X}$	-0.5 to 6V
$V_{SS\_X} – V_{SS\_Y}$	max 0.5V
$V_{DD\_X} – V_{DD\_Y}$	max 0.5V
Voltage on any pin wrt to V_{SS_X}	-0.5 to V_{DD_X}+0.5V
Junction Temperature (Tj)	250°C

ESD Rating

Human Body Model	>2KV

Operating Conditions

Supply Voltage V_{DD_X} to V_{SS_X}:	4.5V to 5.5V
Junction temperature	-55°C to +225°C

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability. Permanent uses of the device in short-circuit state or in over-temperature state may affect long term reliability of the device.*

DC Electrical Characteristics

Unless otherwise stated, T_j = 25°C, $V_{DD\_D}/V_{DD\_A1}/V_{DD\_A2}$=5V. **Bold** figures point out values valid over the whole temperature range (T_j = -55°C to +225°C).

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	$V_{DD\_X} - V_{SS\_X}$		**4.5**	**5**	**5.5**	V
Output voltage range	V_{OUT}		**0**		**5**	V
Quiescent current	I_Q	CLK= '0'; CONFIG= '0' 1 amplifier active, no load		1.2	**2**	mA
Standby current	I_{STDBY}	CLK= '0'; CONFIG= '0', ENABLE = '0'; T_j = 25°C		1.5		µA
		CLK= '0'; CONFIG= '0', ENABLE = '0'; T_j = 225°C			7	µA
Internal clock frequency	F_{INT}	CLK= '0'; CONFIG= '0'; T_j = 25°C		360		kHz
Output voltage swing	V_O	RL=250Ω	**0.35**		**VDD -0.4**	V
		RL=1kΩ	**0.09**		**VDD -0.1**	V
		RL=∞	**0.01**		**VDD - 0.01**	V
Max Output current[1,2]	I_O	T_j=25°C	20			mA
		T_j=225°C	**15**			mA
Output short-circuit current	I_{SC}			100		mA
External output capacitance					**200**	pF
Common mode input range	V_{CM}		**0.1**		**VDD -0.1**	V
Input offset voltage	V_{IOFF}	T_j=25°C		50		µV
		T_j=225°C			**100**	µV
Input offset drift	TC_{VIOFF}	Maximum variation over [-40-175]°C temperature range			**90**	µV
Input leakage current	I_B	T_j=25°C, CMInput = 2.5V		±7		pA
		T_j=225°C, CMInput = 2.5V		±50		nA
Input offset current	I_{OFF}	T_j=25°C		±14		pA
		T_j=225°C		±120		nA
Input capacitance	$C_{IN,DIFF}$	Differential, CMInput = 2.5V		1.5		pF
	$C_{IN,CM}$	Single-ended, CMInput = 2.5V		3		pF
Open-loop output impedance		Io=0mA, f=3MHz, Av=+1	150	250	400	Ω
Thermal resistance	θ_{JC}			11		°C/W
	θ_{JA}	pad area = 1 cm^2		80		°C/W

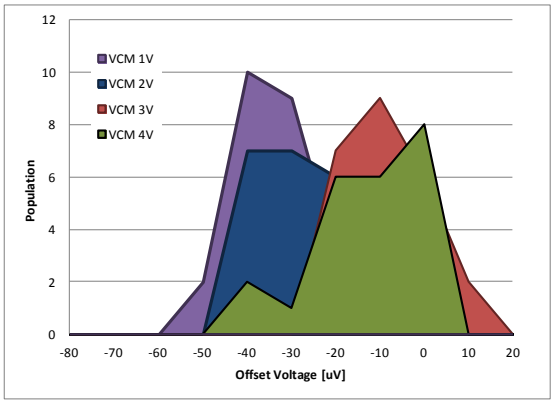
[1] Source or sink.
[2] Output current is not internally limited. Value given indicates the maximum recommended conditions.

AC Electrical Characteristics

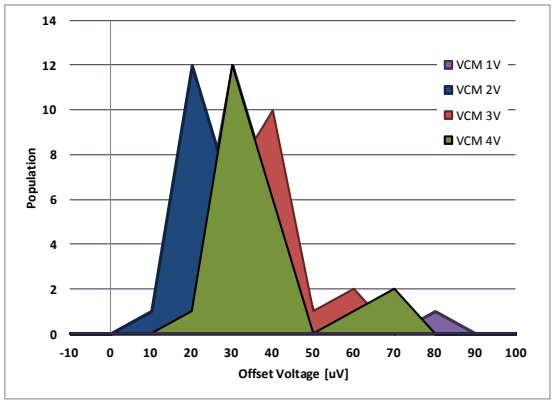
Unless otherwise stated, T_j = 25°C, $V_{DD\_D}/V_{DD\_A1}/V_{DD\_A2}$=5V. **Bold** figures point out values valid over the whole temperature range (T_j = -55°C to +225°C).

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DC open-loop gain	A_O	RL=2kΩ, T_j=25°C, CMInput = 2.5V		85		dB
		RL=2kΩ, T_j=225°C CMInput = 2.5V		85		dB
Gain-bandwidth product	GBW	RL=2kΩ, CL=30pF, T_j=25°C CMInput = 2.5V	2.2	2.8		MHz
		RL=2kΩ, CL=30pF, T_j=225°C CMInput = 2.5V	2.5	3.6		MHz
Common mode rejection ratio	CMRR	DC to 1kHz, T_j=25°C	85	105		dB
		DC to 1kHz, T_j=225°C	88	99		dB
Power supply rejection ratio	PSRR	Positive or negative. DC to 100Hz, T_j=25°C CMInput = 2.5V		95		dB
		Positive or negative. DC to 100Hz, T_j=225°C CMInput = 2.5V		95		dB
Slew rate	SR	RL=2kΩ, CL=30pF, T_j=25°C	1.9	2.7		V/µs
		RL=2kΩ, CL=30pF, T_j=225°C	3	4		
Phase margin	Φ_M	RL=2kΩ, CL=30pF, T_j=25°C	35	41		°
		RL=2kΩ, CL=30pF, T_j=225°C	27	32		°
Input noise spectral density	e_{sd}	F=10Hz		0.3		µV/√Hz
		F=100Hz		0.3		
		F=1kHz		0.3		
		F=10kHz		0.09		
Integrated input noise voltage	e_{ni}	0.1 Hz to 10Hz		5		μV_{pp}
Input noise current		10Hz		TBD		fA/√Hz

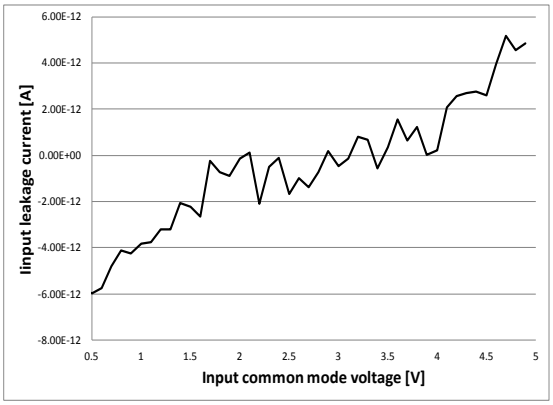
Typical Performance Characteristics



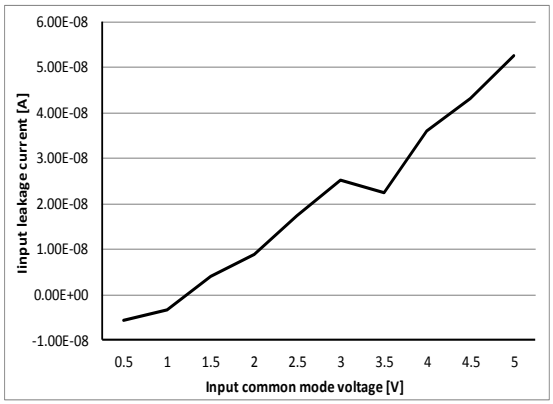
Input Offset distribution (VDD=5V, T=25°C) (VCM= Input common mode voltage)



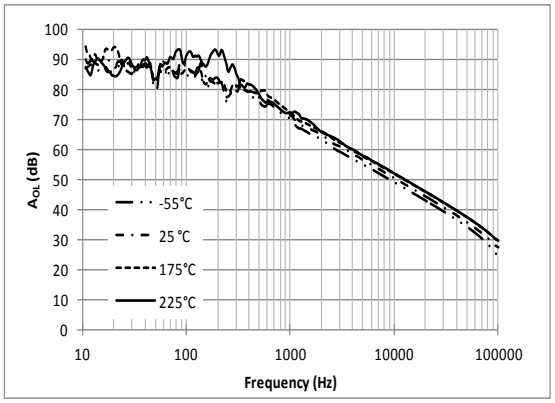
Input Offset maximum thermal drift over [-40°C-175°C] temperature range (VDD=5V)



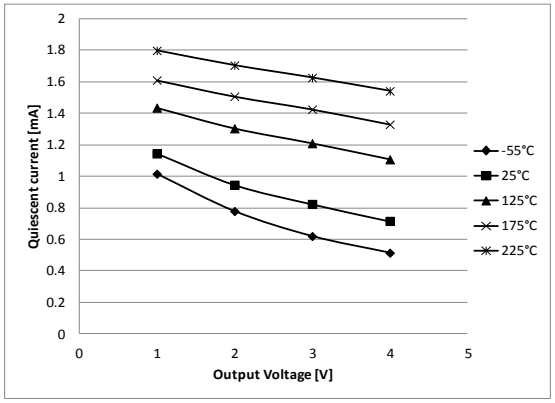
Input leakage current vs input common mode voltage (25°C)



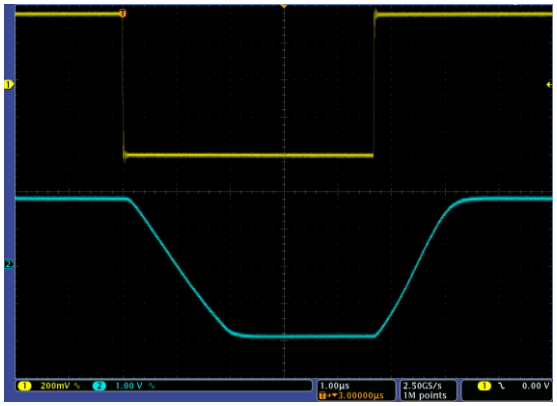
Input leakage current vs input common mode voltage (225°C)



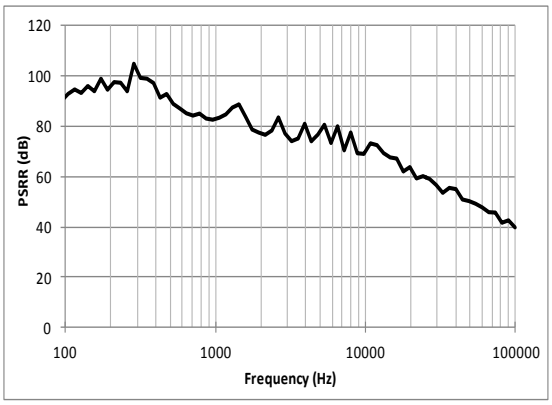
Open loop Gain vs Frequency (no load)



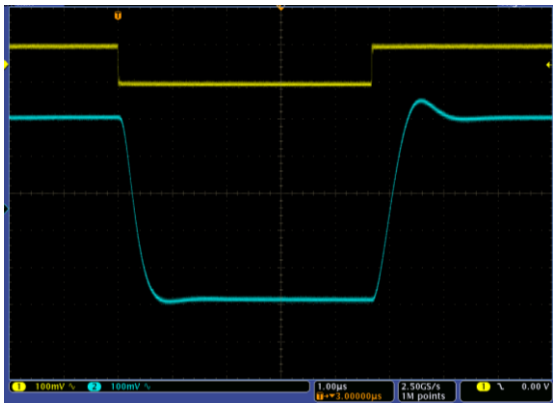
Supply current vs temperature



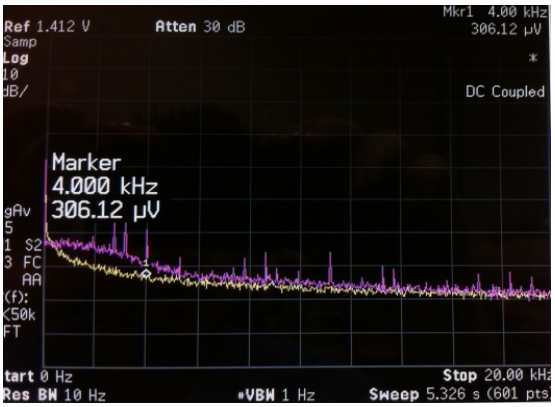
Large signal transient response (swing= 1V,gain =5, Cl= 220pF)



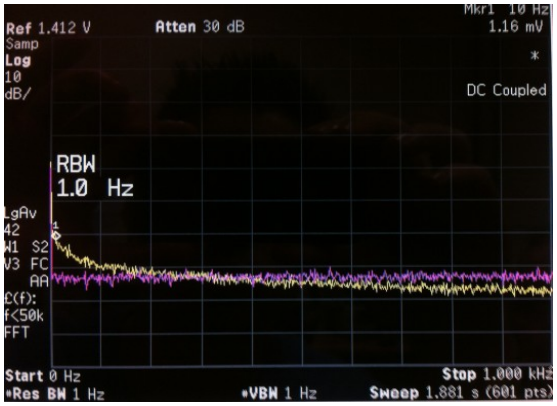
PSRR vs Frequency



Small signal transient response (swing= 100mV,gain =5, Cl= 220pF)



Voltage noise Density from 0.1Hz to 20 KHz (purple: with compensation; yellow: without compensation) (real value = measured value – 60dB)



Voltage noise Density from 0.1Hz to 1 KHz (purple: with compensation; yellow: without compensation) (real value = measured value – 60dB)

Circuit Functionality

Architecture

CHT-OPAL implements two low-noise, low-offset operational amplifier cells.

The amplifiers implement a proprietary compensation architecture for automatic offset correction and low-frequency noise improvement on the whole temperature range. As the use of a compensation clock generates unavoidable clock ripple on the output signal, and even though special care has been taken to the circuit design in order to minimize this ripple, the user may need to filter it externally. CHT-OPAL offers several configuration options in order to bring maximum flexibility to the user in regards to filtering: The clock operation can implement a spread spectrum function, which allows minimization of the output ripple amplitude on the clock frequency, the noise (ripple) energy being spread on the harmonics. Alternatively, the spread spectrum function can be disabled, in which case 100% of the ripple will be concentrated on the clock frequency. This later option is more suitable when external filtering (notch filter) or synchronization with external sampling devices is implemented.

Secondly, OPAL's offset compensation block can run either from an internal clock or from an external clock; the latter allows external synchronization and will typically be used by sampled systems (e.g. ADC). Use of the internal clock operation does not require any dedicated external components (e.g. capacitance). Selection of the external clock frequency can be made within a very wide range of 12 KHz to 500 KHz: the user will find an adequate frequency outside the useful bandwidth in most instrumentation and sensing applications.

When the spread spectrum function is enabled, CHT-OPAL compensation circuitry operates with a pseudo-random clock (generated from the master internal or external clock). This pseudo-random clock is generated by a 32-to-64 divider of the master clock (5.5 KHz to 11 KHz typ. When generated from the internal clock). This spreads the clock noise over a frequency octave.

CHT-OPAL also features a shutdown mode where the 2 Op Amps are inactive; the circuit is then in its lowest power consumption mode, with only a few µA drawn from the power supply.

External gain setting

CHT-OPAL is intrinsically stable for gain higher 3V/V. For gain lower than 3V/V, an external compensation network should be added. The network shown on Figure 1 stabilizes CHT-OPAL in unitary gain configuration and reduces its bandwidth by a factor 6.

Table below summarizes the different gain configurations.

Gain (G) [V/V]	Max output capacitance	External compensation network
G > 5	200pF	Not needed
3 < G < 5	50pF	Not needed
G < 3	50pF	Needed as shown on Figure 1

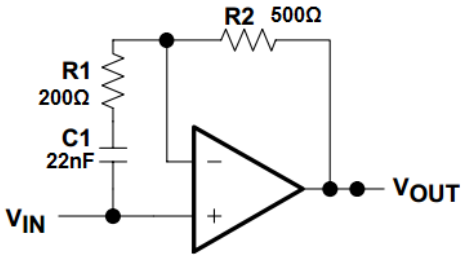


Figure 1

CHT-OPAL can also support higher output capacitance, with additional compensation network. Contact CISSOID for more information.

Modes of operation

OPAL's behavior is controlled by 3 configuration pins. Table1 below summarizes the 5 different modes of operation.

CLK	CONFIG	ENABLE	MODE	OPERATION
X	X	0	MODE1	Standby mode
0	0	1	MODE2	Internal oscillator;spreadspectrum enabled
CLK > 9kHz	0	1	MODE3	External clock;spreadspectrum enabled
1	0	1		Internal test mode
0	1	1	MODE4	Internal oscillator;spreadspectrum disabled
CLK > 9kHz	1	1	MODE5	External clock;spreadspectrum disabled
1	1	X		Internal test mode

MODE1:

By setting the pin ENABLE to "0", OPAL is put in standby mode where current consumption is reduced to a few µA. When OPAL is in that mode, the 2 outputs are in High Impedance state.

MODE[2..5]:

Those 4 modes are standard modes of operation for OPAL. They differ by the way the internal auto-zero control signals are internally generated.

If CLK pin is put to "0", the master clock is generated by an internal oscillator (Fosc = 360 KHz typ.).
Whenever OPAL' internal circuitry senses an external clock signal with a frequency higher than 9KHz applied on the CLK pin, the circuits operates automatically in external clock mode, using CLK signal as the master clock.

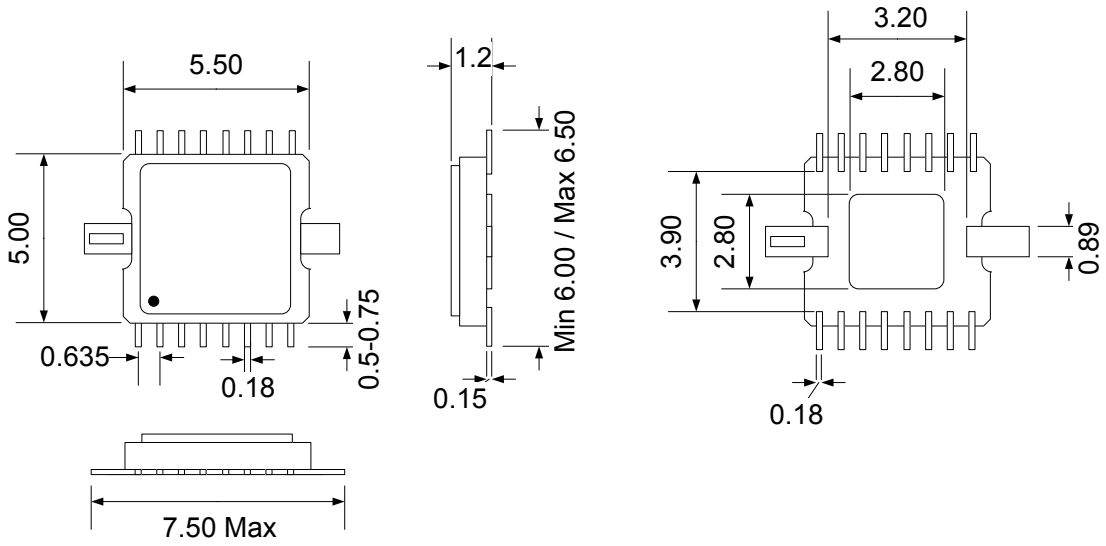
With the CONFIG pin, one can configure OPAL to use the spread spectrum function to generate the internal auto-zero control signals

Choice of one of those 4 modes depends on the application constraints (signal useful band, synchronization with external devices…).

Single OPA

If the application only requires a single operational amplifier, the OPAL current consumption can be optimized by connecting VDD_A1 or VDD_A2 to respectively VSS_A1 or VSS_A2.

Package Dimensions (TDFP16)



Physical dimensions (mm +/- 10%)

Ordering Information

Product Name	Ordering Reference	Package	Marking
CHT-OPAL	CHT-GEM6489A-TDFP16-T	TDFP16	CHT-GEM6489A

Contact & Ordering

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