CMT-HADES2S Preliminary Datasheet

Version: 1.7
27-Jan-22
(Last Modification Date)

High Temperature Gate Driver - Secondary Side IC: Driver & Protection Functions

General description

CMT-HADES2S is a high-temperature, high reliability single chip fully integrated gate driver specifically designed to drive wide-bandgap high voltage / high power transistors, in particular Gallium Nitride (GaN) and Silicon Carbide (SiC) devices. It offers the most compact solution available on the market thanks to its small size and the low number of external components it requires, It also features the highest output current in the industry for products of this type. CMT-HADES2S can be used with standard silicon MOSFETs and IGBTs in extended temperature applications (>125°C) where it brings an increase in reliability and lifetime by an order of magnitude compared to traditional solutions. The circuit features push-pull transistors capable of sourcing/sinking up to 12A each. It includes as well soft-shutdown, under-voltage lockout, desaturation detection, Active Miller Clamping, over-temperature sensing and isolation interface to primary function.

CMT-HADES2S can be used either stand-alone or in combination with CMT-HADES2P, which generates control signal to drive high bandwidth transistors.

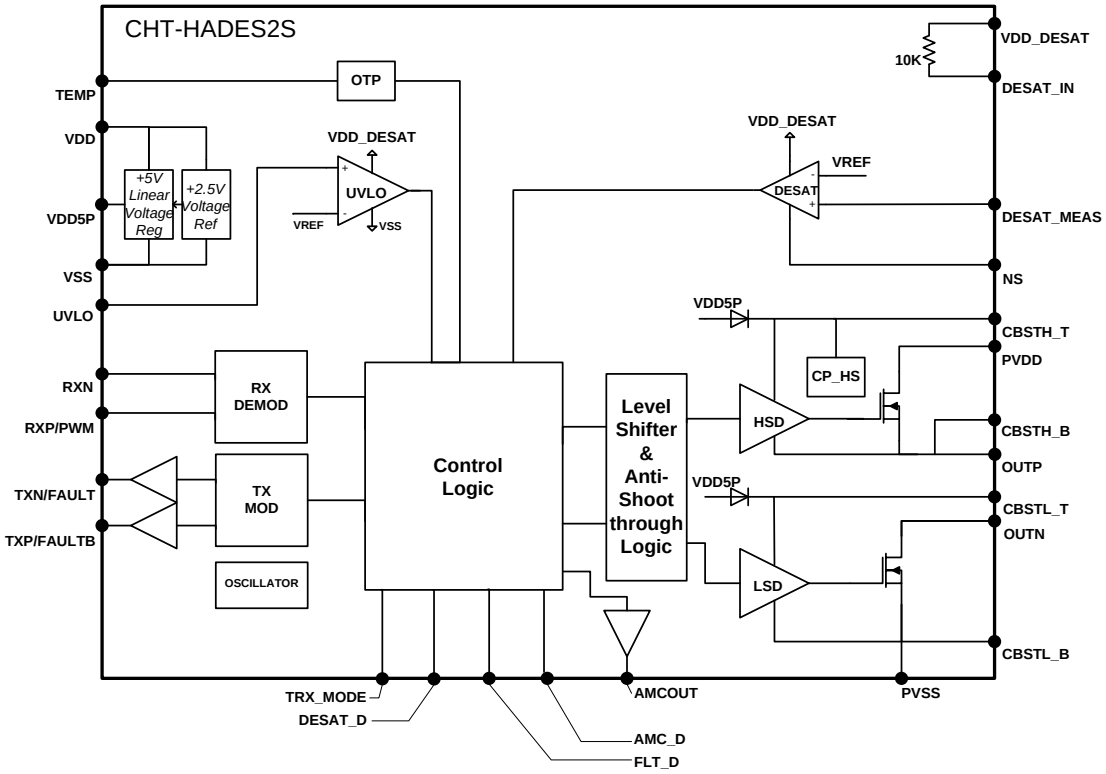
Applications

- Ideally suited for high reliability markets like automotive, aerospace, railway, Oil & Gas
- Motor drivers : electrical cars, railway, industrial pumps, down-hole,…
- Actuators
- DC-DC converters and SMPS : battery chargers, …
- Inverters : olar inverters, smart grid, EV and HEV, 3 phases inverters
- Power conversion : uninterruptible power supplies, wind turbine, …

Features

- Operating junction temperature:
  - from -55°C to +175°C
- Supply voltage: 5 to 30V
- Output peak current:
  - 12A @ 125°C
  - 9A @ 175°C
- RDS_{ON}:
  - 0.25Ω typ. @ 25°C
  - 0.45Ω typ. @ 175°C
- Max PWM frequency : 1MHz
- Propagation delay: 160 ns typ.
- Rise time / fall time (C_{Load}=1nF):
  - 30ns typ
- Isolated OOK modulated interface:
  - 1 TX and RX channels
- Standard digital interface (PWM, FAULT)
- Soft-shut down
- Desaturation detection w/ programmable threshold & blanking time
- Under-Voltage Lockout (UVLO)
- Over temperature protection
- Fault generation with programmable automatic re-start timer
- Active Miller Clamping (w/ ext. MOSFET)
- Common mode transient immunity:
  - >50kV/µs typ.
- Capable to drive wide variety of power switch types
- Package: Plastic PQFP44

Functional Block Diagram

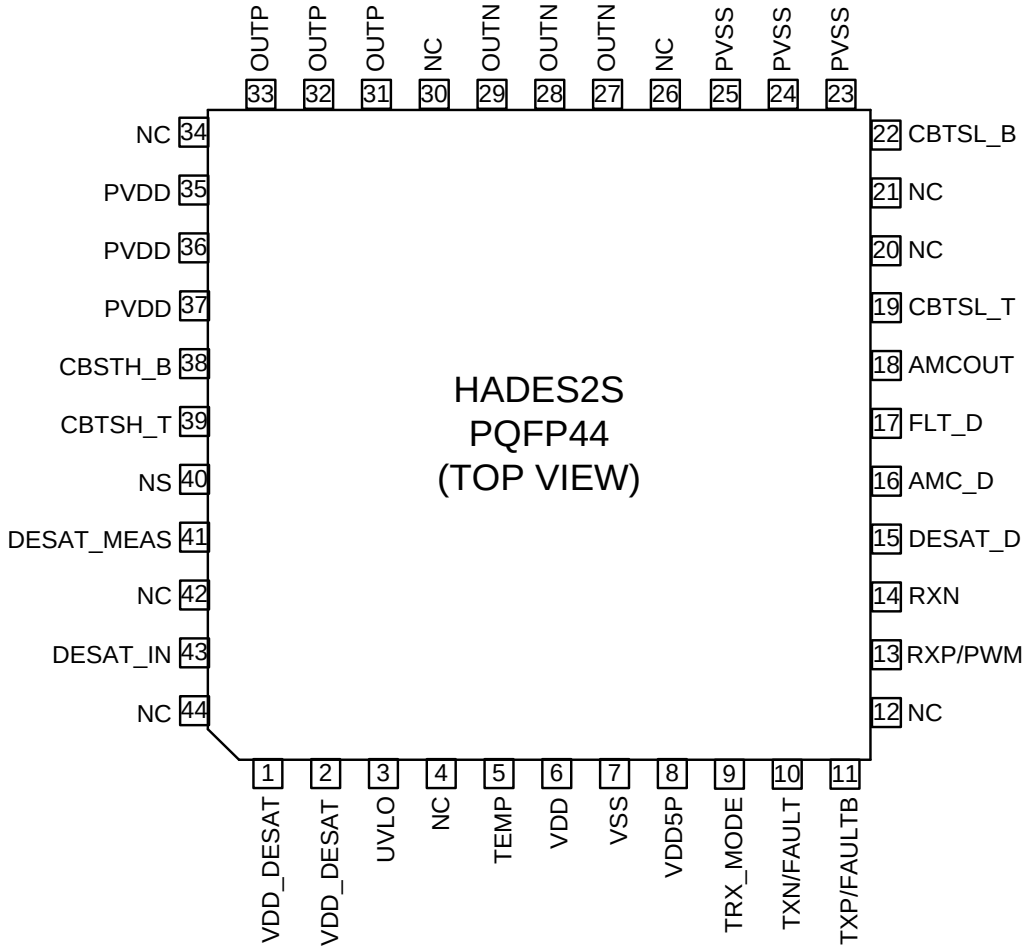


Pin Description:[1]

Pin #	Pin Name	Pin Description
1,2	VDD_DESAT	DESAT/UVLO function power supply: - Connect to PVDD for MOSFET/Normally Off/BJT/IGBT - Connect typ. to +15V for Normally On
3	UVLO	UVLO (Under Voltage Lockout) input Internally compared with VREF(2.5V)
5	TEMP	Temperature sensor open drain output
6	VDD	Voltage reference and 5V voltage regulator positive power supply
7	VSS	Device negative power supply
8	VDD5P	5V internal voltage regulator output (referenced to VSS); connect to decoupling capacitor (typ. 1 µF)
9	TRX_MODE	Select transmission mode towards primary side (internal pull-down): “0”: modulated control interface “1”: standard digital interface (PWM/FAULT)
10	TXN/FAULT	Negative differential output; to be connected to the primary of the pulse transformer. or FAULT digital output signal (push-pull)
11	TXP/FAULTB	Positive differential output; to be connected to the primary of the pulse transformer or FAULTB digital output signal (push-pull)
13	RXP/PWM	Positive differential input; to be connected to the secondary of the pulse transformer or PWM digital Schmitt trigger input
14	RXN	Negative differential input; to be connected to the secondary of the pulse transformer.
15	DESAT_D	Set DESAT blanking period duration. Connect capacitor to this pin to program blanking duration
16	AMC_D	Set AMC (Active Miller Clamp) delay. Connect capacitor to this pin to program AMC delay
17	FLT_D	Set the Fault reset delay. Connect capacitor to program delay; When fault has been detected, driver is turned-off for a period of time defined by FLT_D
18	AMCOUT	Active Miller Clamp (AMC) output signal (to control an external AMC transistor)
19	CBSTL_T	Top plate of low-side bootstrap capacitor
22	CBSTL_B	Bottom plate of low-side bootstrap capacitor
23,24,25	PVSS	Negative power supply of Low Side output MOS: - Connect to -5V for MOSFET - Connect to -15V for Normally Off/Normally On - Connect to [-15,0]V for IGBT
27,28,29	OUTN	Sinking output
31,32,33	OUTP	Sourcing output
35,36,37	PVDD	Positive power supply of High Side output MOS: - Connect typ. to +20V for MOSFET - Connect typ. to +15V for Normally Off JFET/BJT/IGBT - Connect to 0V for Normally On JFET
38	CBSTH_B	Bottom plate of high-side bootstrap capacitor
39	CBSTH_T	Top plate of high-side bootstrap capacitor
40	NS	External FET source voltage; used by DESAT comparison function
41	DESAT_MEAS	DESAT sensed input; internally compared to VREF (2.5V)
43	DESAT_IN	Can feed of the desaturation sensing diode

[1] Not connected pins (NC) are not listed in the Pin Description table; those pins are not connected internally and can be left floating or connected to any net to ease PCB routing

Pinout:[2]



[2] NC: not connected internally

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
(VDD-VSS/PVDD-PVSS)	-0.5	35	V
(VDD_DESAT-VSS,NS-VSS)	-0.5	35	V
(VDD5P-VSS), (CBTSL_T-CBTSL_B), (CBTSH_T-CBTSH_B)	-0.5	6	V
CBTSH_T	PVSS-0.5	PVDD+5.5	V
CBTSL_T	PVSS-0.5	VDD5P+0.5	V
AMCOUT, TXP/FAULT, TXN/FAULTB, TRX_MODE, AMC_D, DESAT_D, RXP/PWM, RXN, FLT_D, TEMP	VSS-0.5	VDD5P+0.5	V
DESATIN, DESAT_MEAS	NS-0.5	VDD_DESAT+0.5	V
OUTN, OUTP, CBTSH_B	PVSS-0.5	PVDD+0.5	V
CBTSL_B	PVSS-0.5	PVSS+0.5	V
UVLO	VSS-0.5	VDD_DESAT+0.5	V
Junction Temperature		190	°C
ESD Rating (Human Body Model)	1		kV
Max power dissipation		1.25	W

Operating conditions

Parameter	Min.	Max.	Units
(PVDD-PVSS)	0	30	V
(VDD_DESAT,NS-VSS)	0	30	V
(VDD-VSS)	7	VDD_DESAT-VSS	V
(VDD5P-VSS), (CBTSL_T-CBTSL_B), (CBTSH_T-CBTSH_B)	0	5.5	V
CBSTH_T	PVSS	PVDD+5	V
CBSTL_T	PVSS	VDD5P	V
AMC_OUT, TXP/FAULT, TXN/FAULTB, TRX_MODE, AMC_D, DESAT_D, RXP/PWM, RXN, FLT_D, TEMP	VSS	VDD5P	V
DESATIN, DESAT_MEAS	NS	VDD_DESAT	V
OUTN, OUTP, CBTSH_B	PVSS	PVDD	V
CBTSL_B	PVSS	PVSS	V
UVLO	2.5V	VDD_DESAT	V
Junction Temperature		175	°C
Max power dissipation		1	W

Parameter	Condition	Min	Typ	Max	Units
Thermal resistance					
$R_{\Theta JA}$: junction–to-air thermal resistance	Mounted on PCB; no thermal pad at PCB level; still air; devices in horizontal or vertical position		55		°C/W

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

Electrical Characteristics

Unless otherwise stated: VDD/VDD_DESAT/PVDD-VSS/PVSS)=25V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +175°C).

Parameter	Condition	Min	Typ	Max	Units
External Power Supply					
External Power Supply VDD/VDD_DESAT/PVDD	Versus VSS	7[3]		30	V
I_Q(VDD)	RXN, RXP/PWM=0 No external load connected to VDD5P MOSFET configuration No fault situation		9.2		mA
I_Q(VDD_DESAT)	«RD1_I+RD2_I» = 250KΩ No external resistors Excluding current through the DESAT high voltage diode		0.9		mA
I_{AVG}(PVDD)	20kHz, 50% duty cycle VDD/PVDD/VDD_DESAT-VSS = 25V Q_{LOAD} = 90nC, Rg = 5Ω MOSFET configuration No fault situation		2.3		mA
I_{AVG}(VDD)			9.6		mA
I_{AVG}(VDD_DESAT)			0.9		mA
I_{AVG}(PVDD)	20kHz, 50% duty cycle VDD/PVDD/VDD_DESAT-VSS = 25V Q_{LOAD} = 90nC, Rg = 5Ω MOSFET configuration Fault situation		0.15		µA
I_{AVG}(VDD)			1.8		mA
I_{AVG}(VDD_DESAT)			0.9		mA
5V Power Supply					
Internal 5V Power Supply (VDD5P) versus VSS	(VDD-VSS) from 7V to 30V, Iout from 0.25mA to 30 mA	**4.75**	5	**5.25**	V
Output Capacitor		**1000**			nF
	ESR		100		mΩ
Output Current	Including internal consumption (11.9mA consumed by the device in normal operation)	**0.25**		**30**	mA
Initial Accuracy	Iout=2.5mA; Tj=25°C		+/-2		%
Drift with temperature	Iout=2.5mA		-0.4		mV/°C
Line Regulation	(VDD-VSS) from 7V to 30V; Iout=2.5mA		+/-0.1		%
Load Regulation	Iout from 2.5mA to 25mA		-1.25		%

[3] If regulator is bypassed, it is possible to use the device with a 5V supply (see Device power supplies and decoupling scheme section [page 18])

Electrical Characteristics

Unless otherwise stated: (VDD/VDD_DESAT/PVDD-VSS/PVSS)=25V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +175°C).

Parameter	Condition	Min	Typ	Max	Units
Input signal (RXP/PWM, RXN)					
Minimum HIGH level input voltage V_{IH}	**TRX_MODE = 1** RXP/PWM signal	**3.0**	3.4	**3.8**	V
Maximum LOW level input voltage V_{IL}		**1.3**	1.6	**2.05**	V
Hysteresis		**1.4**	1.8	**2.4**	V
Impedance	**TRX_MODE = 0** Between RXP & RXN/VSS Between RXN & RXP/VSS	**2**	3	**4**	kΩ
Common mode transient immunity	0.5 pF pulse transformer parasitic capacitor	**50**			KV/µS
Output signals (TXP/FAULT, TXN/FAULTB) (TRX_MODE = 1)					
Minimum HIGH level output voltage V_{OH}	I_{OH} < 8mA (source)	**4.4**			V
Maximum LOW level output voltage V_{OL}	I_{OI} < 8mA (sink)			**0.63**	V
Output Rise/Fall Time (10% to 90%)	On 50 pF external capacitor		10		ns
Output signals (TXP/FAULT, TXN/FAULTB) (TRX_MODE = 0)					
High state output resistance			20		Ω
Low state output resistance			23.5		Ω
Modulation frequency			15		MHz
Modulation frequency variation	Includes process/ temperature/power supply variations	**-35**		**+40**	%
Modulation frequency duty cycle	Includes process/ temperature/power supply variations	**48.5**		**51.5**	%
Drivers					
OUTN sink peak current		**8**	12		A
OUTN sink avg current				**1.5**	A
OUTP source peak current		**8**	12		A
OUTP source avg current				**1.5**	A
High state output resistance			0.3	**0.45**	Ω
Low state output resistance			0.3	**0.45**	Ω
Rise Time (10%-90%)	Cload=1nF; Rg = 5Ω		30		ns
Fall Time (10%-90%)	Cload=1nF; Rg = 5Ω		30		ns
Soft Shut-down (SSD)					
SSD switch ON-Resistance			35		Ω
PWM path					
Switching frequency				**1000**	kHz
Duty cycle		**0**		**100**	%
Propagation delay when output rising (RXP/PWM →OUTP)	(VDD-VSS)=15V (50%→ 10%) TRX_MODE= 0		150		ns
Propagation delay when output falling (RXP/PWM →OUTN)	(VDD-VSS)=15V (50%→ 90%) TRX_MODE= 0		165		ns
Propagation delay when output rising (RXP/PWM →OUTP)	(VDD-VSS)=15V (50%→ 10%) TRX_MODE= 1		121		ns
Propagation delay when output falling (RXP/PWM →OUTN)	(VDD-VSS)=15V (50%→ 90%) TRX_MODE= 1		101		ns
Jitter (RMS cycle-2-cycle)	RX path (from RXP/RXN to OUTP/OUTN) TRX_MODE= 0			**10**	ns

Electrical Characteristics (continued)

Unless otherwise stated: VDD/VDD_DESAT/PVDD-VSS/PVSS)=25V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +175°C).

Parameter	Condition	Min	Typ	Max	Units
Under-voltage Lockout (UVLO)					
UVLO comparison threshold		**2.5**	2.6	**2.7**	V
UVLO threshold variation with temperature			-0.17		mV/°C
UVLO hysteresis internal resistance		**36**	50	**62**	kΩ
Delay from UVLO detection to UVLO fault			180		ns
Delay from UVLO detection to OUTN/OUTP output disable	Through Soft Shutdown Cload=1nF		260		ns
Active Miller Clamping (AMC) Pre-driver					
AMC delay range t_{AMC} range	C_{AMC_D} from 5.6pF to 75pF	200		1400	ns
AMC delay variation	Excluding variation on external capacitor	-25		+25	%
AMCOUT voltage swing		**0**		**VDD5P**	V
AMCOUT high state Ron			30		Ω
AMCOUT low state Ron			30		Ω
AMCOUT Rise Time (10%-90%)	CLoad=0.5nF		40		ns
AMCOUT Fall Time (10%-90%)	CLoad=0.5nF		40		ns
Delay “AMCOUT fall 10%” to “OUTP rise 10%”		**20**			ns
DESAT detection					
Blanking time t_{DESAT_D} range	C_{DESAT_D} from 7.15pF to 562pF	0.2		7.8	µs
Blanking time variation	Excluding variation on external capacitor	-25		+25	%
DESAT supply resistance Rs			10		kΩ
DESAT comparison threshold	Wrt to NS node	**2.4**	2.65	**2.9**	V
DESAT threshold variation with temperature			-0.34		mV/°C
DESAT comparator propagation delay				**TBD**	ns
Delay t_{FL_DESAT} between DESAT detection and OUTN/OUTP output disable	Through Soft Shutdown CLoad=1nF After t_{DESAT_D} time		300		ns
Over Temperature protection					
Over temperature protection Threshold (TH_{OTP})	Low to High temperature variation		300		°C
Over temperature protection Hysteresis ($Hyst_{OTP}$)			30		°C
TEMP open drain ON-resistance			140		Ω
Fault latching time					
Timer range t_{FLT_D}	C_{FLT_D} from 20pF to 1µF	**0.01**		**500**	ms
Timer variation	C_{FLT_D} = 20 nF; excluding external capacitor spread	**8**	10	**13**	ms

Typical Performance Characteristics

Unless otherwise stated: VDD/VDD_DESAT/PVDD-VSS/PVSS)=25V

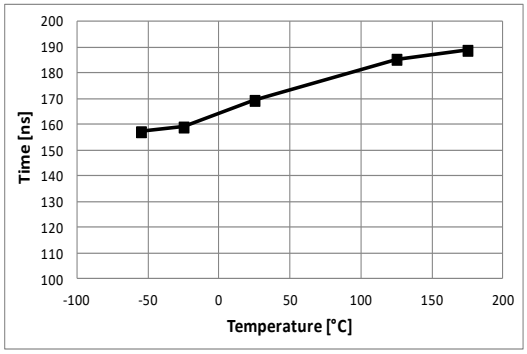


Figure 1: Turn-Off propagation delay (from 50% RXP/PWM to OUT 90%; Cload = 1nF; TRX_MODE=0)

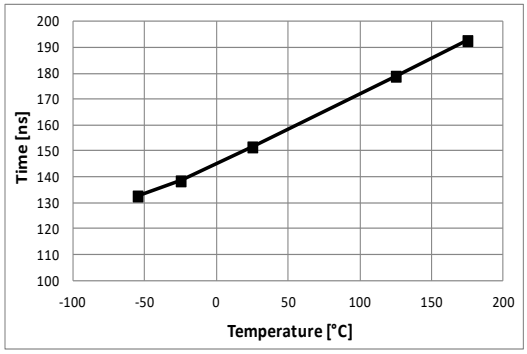


Figure 2: Turn-On propagation delay (from 50% RXP/PWM to OUT 10%; Cload = 1nF; TRX_MODE=0)

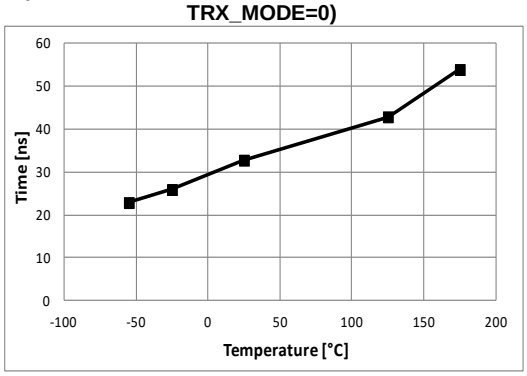


Figure 3: Turn-Off fall time (Cload = 1nF; Rg= 5Ω; PVDD-PVSS=25V)

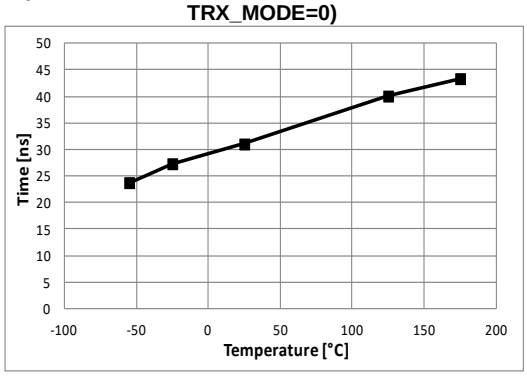


Figure 4: Turn-On rise time (Cload = 1nF; Rg= 5Ω; PVDD-PVSS=25V)

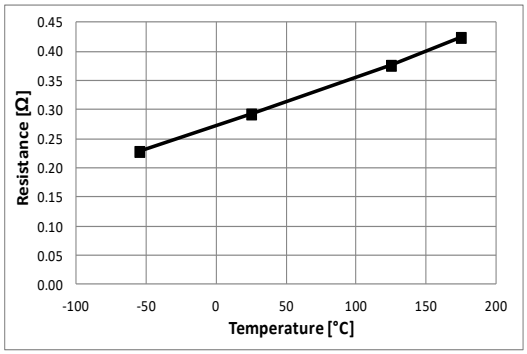


Figure 5: Low-side output resistance

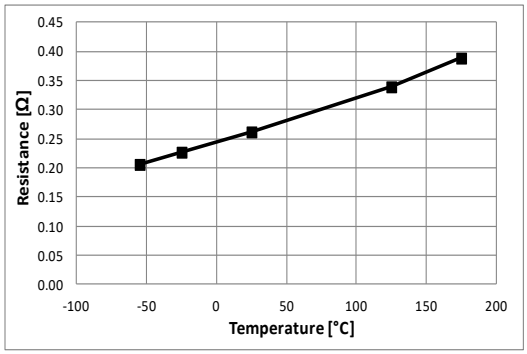


Figure 6: High-side output resistance

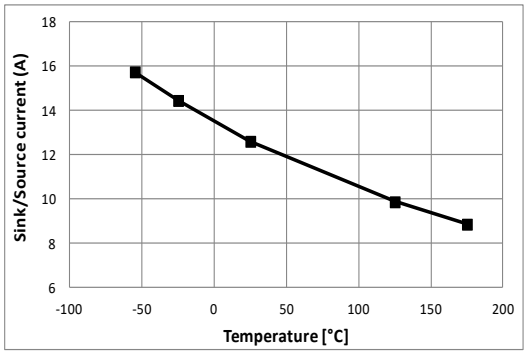


Figure 7: Peak sink/source current

Typical Performance Characteristics (cnt'd)

Unless otherwise stated: VDD/VDD_DESAT/PVDD-VSS/PVSS)=25V

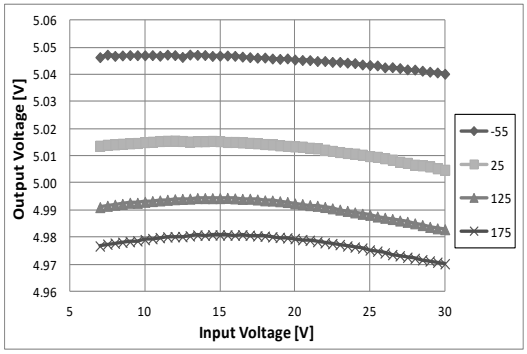


Figure 8: Voltage regulator line regulation ((VDD-VSS) from 7V to 30V; Iout=2.5mA)

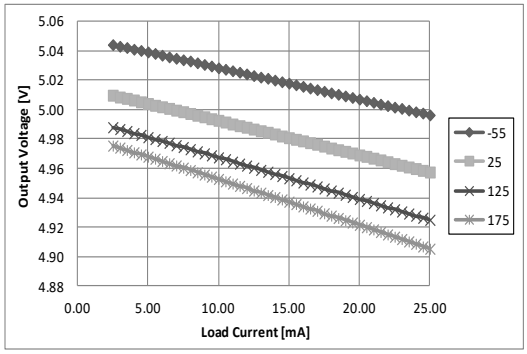


Figure 9: Voltage regulator load regulation (Iout from 2.5mA to 25mA; (VDD-VSS)= 25V)

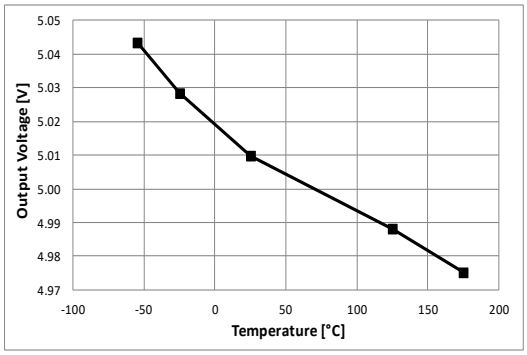


Figure 10: Voltage regulator (Iout from 2.5mA; (VDD-VSS)= 25V)

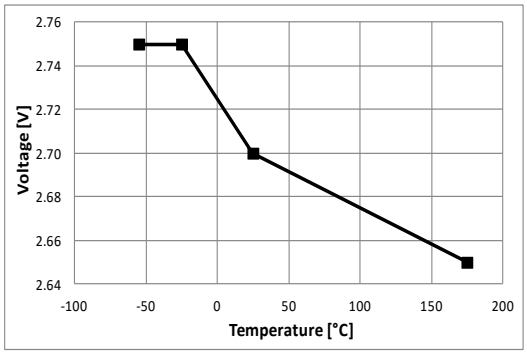


Figure 11. DESAT threshold

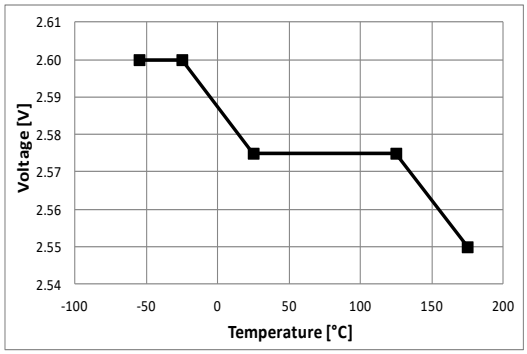


Figure 12. UVLO threshold

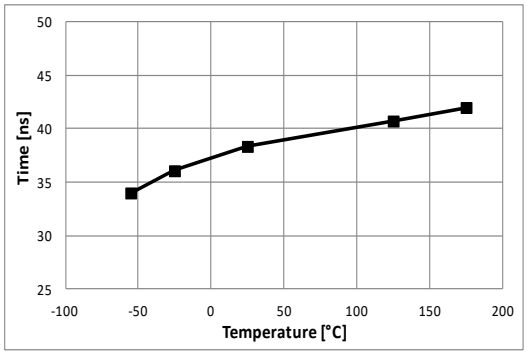


Figure 13. AMCOUT rise time (Cload on AMCOUT: 0.5 nF)

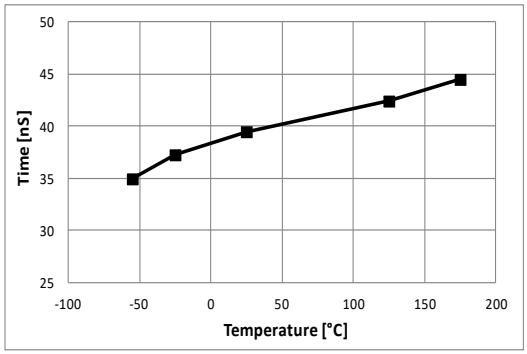


Figure 14. AMCOUT fall time (Cload on AMCOUT: 0.5 nF)

Typical Performance Characteristics (cnt'd)

Unless otherwise stated: VDD/VDD_DESAT/PVDD-VSS/PVSS)=25V

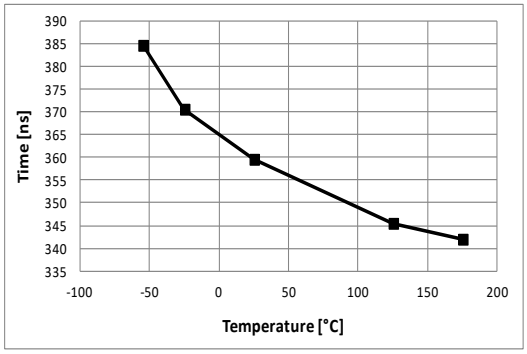


Figure 15. tAMC delay
(CAMC_D=20pF incl. parasitics)

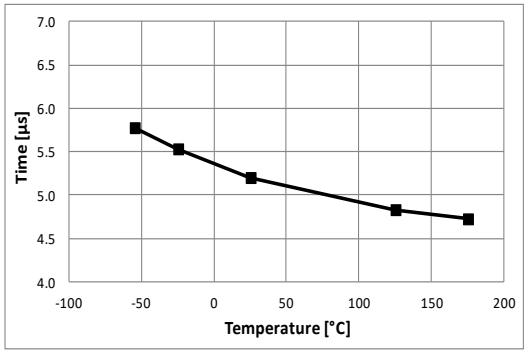


Figure 16. tDESAT_D delay
(CDESAT_D=340pF incl. parasitics)

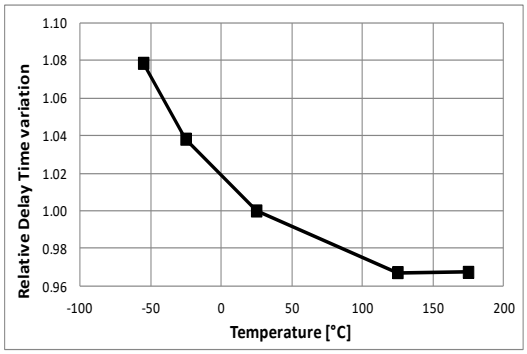


Figure 17. tFLT_D delay
(CFLT_D=20nF)

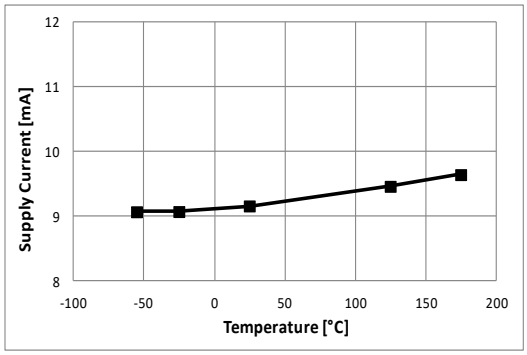


Figure 18. Quiescent current I_q(VDD)
(0 Hz; no fault; [VDD-VSS]=25V)

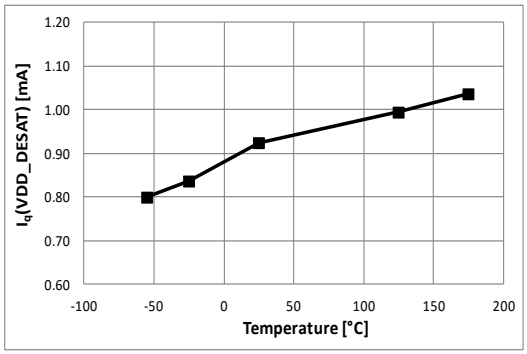


Figure 19. Quiescent current I_q(VDD_DESAT)
(any PWM frequency; fault or no fault state;
[VDD_DESAT-VSS]=25V)

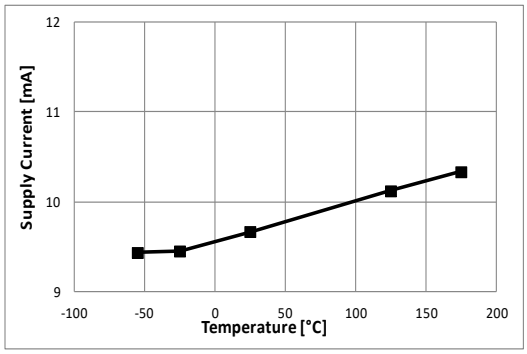


Figure 20. Quiescent current I_q(VDD)
(20 kHz; no fault; [VDD-VSS]=25V)

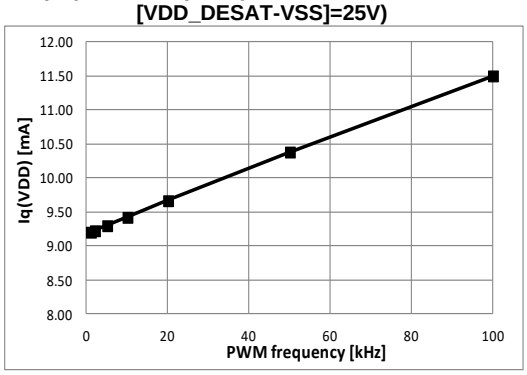


Figure 21. Quiescent current I_q(VDD)
(T=25°C; no fault; [VDD-VSS]=25V)

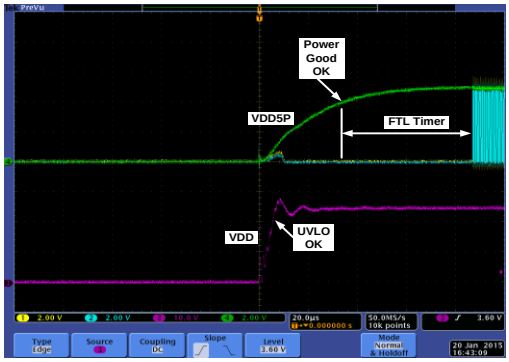


Figure 22. Start-up sequence
(1/2: TX/TXN outputs; 3: VDD; 4: VDD5P)

Circuit functionality

General description

CMT-HADES2S is a high-temperature, high reliability, single-die high power transistor gate driver. Its main features are:

- Sink/source current up to 12A through low-ohmic on-chip transistor (typ. 0.25Ω) enabling fast drive of high power switches (> 200A) with low on-chip power dissipation
- Isolated data transmission (robust to high dV/dt) (data and fault) towards primary side
- Digital 5V interface for data and fault (as alternative to isolated data transmission interface)
- Internal 5V voltage regulator powering internal logic and also usable to supply external 5V devices
- Support of Active Miller Clamping (AMC) function through programmable AMC delay and integrated AMC transistor driver
- Programmable fault timer with automatic restart
- Safe start-up sequence through monitoring of the main supply (UVLO) and of the voltage regulator output (through Power-Good function)
- Permanent and programmable Under-Voltage Lockout (UVLO) monitoring on power switch supplies
- Desaturation detection function with programmable threshold protecting power switches in case of abnormal current levels
- Soft-Shutdown integrated transistor and control performing power device graceful shutdown in case of fault and so preventing too high dI/dt in the power stage
- On-chip temperature monitoring of key functions (push-pull stage and voltage regulator)

Under-Voltage Lockout (UVLO)

The aim of this function is to allow the user to specify a threshold voltage for the power supply under which the gate driver is shut down and a fault is reported to the logic part of the system.
The monitored power supply is “VDD_DESAT-VSS”.

The UVLO threshold is defined by means of 2 external resistors (RU1, RU2) connected to the pin UVLO (cfr Figure 23).

To avoid oscillation when (VDD_DESAT-VSS) is close to the UVLO threshold, a hysteresis is implemented internally via a resistor RU3 (shunting RU1 resistor before threshold high is reached).

UVLO thresholds are defined by the following equation:

$$\text{UVLO THR LOW} = 2.6V * \left(\frac{RU2+RU1}{RU1}\right)$$

$$\text{UVLO THR HIGH} = 2.6V * \left(\frac{RU2+(RU1*RU3)/(RU1+RU3)}{(RU1*RU3)/(RU1+RU3)}\right)$$

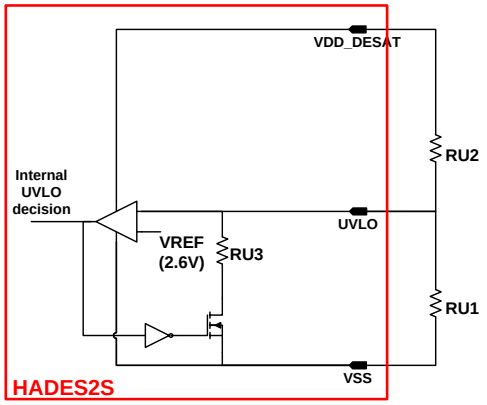


Figure 23: UVLO detection function

Refer to the Fault management chapter for details about fault behavior and management.

Voltage reference and voltage regulator

CMT-HADES2S device includes on-chip voltage reference (2.5V) and also a voltage regulator providing 5V power supply. This 5V supply is used internally by the control interface, the control logic and the pre-drivers of the push-pull stage and can be used to feed external devices.

A 1µF (min) capacitor needs to be connected to the regulator 5V output.

An internal Power-Good function is implemented on the regulator output voltage. Power-Good is considered as OK when output voltage reached 90% of its expected value. This signal is used during start-up phase: when true, it enables transition to normal operation.

Those 2 functions are supplied by the VDD pin. VDD pin supply range extends between 7V (min operating voltage of the voltage reference and linear voltage regulator) and 30V (max operating voltage of the whole device).

VDD supply can be generated by:

- An external dedicated supply
- Connecting VDD pin directly to VDD_DESAT
- Connecting VDD pin to VDD_DESAT via an external resistor

The last option enables to spread the dissipation (due to the linear voltage regulator dropout) between the resistor and the internal linear voltage regulator. For proper sizing of this external resistor, please refer to the section “Device power supplies and decoupling scheme”.

In any case, VDD must lower or equal to VDD_DESAT.

Desaturation detection

The purpose of the DESAT function is to detect that the voltage at the drain of the power switch, in “ON” state, is higher than a given threshold. This informs the logic part of the system about possible damage of the power arm (e.g. a short circuit at the arm level leading to an overcurrent in the power switch).

The sensing of the power device drain voltage is performed through an external high voltage sensing diode whom cathode is connected to the power switch drain and whom anode is connected to DESAT_IN pin. Inside HADES2S device, DESAT_IN pin is connected to VDD_DESAT via a 10KΩ resistor, generating a typ. 1 mA current towards the external sensing diode.

It is also possible to use a resistor as sensing element. System designers should then pay attention to the following aspects:

- Proper isolation needs to be guaranteed between the 2 resistor terminals
- Resistor should have a value in the MΩ range to limit power dissipation
- Power dissipation in the resistor would in any case be significant.

The desaturation threshold is configured by 2 external resistors connected to the pin DESAT_MEAS (cfr Figure 25). Rules to dimension RD1 and RD2 are:

- DESAT threshold == 2.65V*(RD2+RD1)/RD1
- VDD_DESAT*(RD1+RD2)(10K+RD1+RD2) > 1.5 * DESAT threshold

Note that the DESAT function is working between NS and VDD_DESAT power supplies. Considering the DESAT internal threshold voltage of 2.6V (wrt to NS), DESAT_IN threshold can be set at any value between “NS+2.6V” and “VDD_DESAT-1V”.

In the die version of HADES2S, integrated RD1_I/RD2_I offers a default DESAT threshold of 6V (DESAT_PROG needs to be connected to DESAT_MEAS pin).

When the current in the power arm is positive (going out of power arm) and taken by the free-wheeling diode, the voltage on the node “Power device drain” is negative. To avoid a high current path (cfr Figure 24) through the clamping and external DESAT diode, a resistance Rdesatx3 (typ value: 50Ω) is added on the PCB.

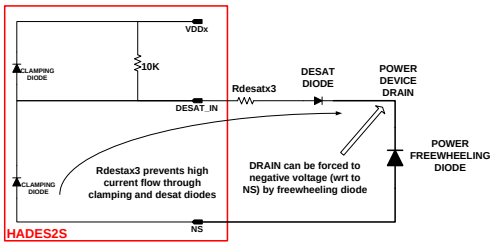


Figure 24: DESAT clamping circuit

At system level, the de-saturation detection should only be taken into account after a defined time following the low-to-high transition on the power device gate. This "blanking" time t_{DESAT_D} is implemented and adjusted by an external capacitor C_{DESAT_D} on the DESAT_D pin and can be calculated as follows:

$$t_{DESAT\_D}\,(ns) = 14 * [C_{DESAT\_D}\,(pF) + 7]$$

In the die version of HADES2S, an integrated capacitor offers a default t_{DESAT_D} of 1µs and can be used by being connected to DESAT_D pad.

The t_{DESAT_D} delay must be higher than the de-saturation comparator delay and must accommodate the time needed by the sensing circuit to reach a steady situation.

If after t_{DESAT_D} time, the DESAT comparator output indicates that DESAT_IN level is higher than the programmed threshold value, an internal DESAT fault is generated. Refer to the Fault management chapter for details about fault behavior and management.

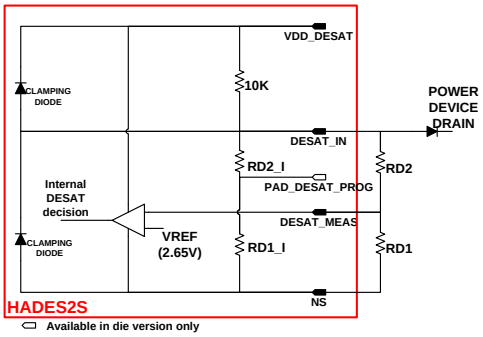


Figure 25: DESAT detection function

The reaction speed of this DESAT detection circuit depends on the parasitic capacitance on node DESAT_MEAS (midpoint RD1/RD2) and the equivalent impedance of RD1 and RD2 in parallel. To get optimal performance, the parasitic capacitance should be minimized on PCB or the value of RD1/RD2 should be adapted.

Active Miller Clamping (AMC)

The purpose of the Active Miller Clamping (AMC) feature is to avoid parasitic cross-conduction (positive kick on VGS) or punch-through (negative kick on VGS) during different switching phases in FET bridge arms (high/low side switches) in the context of power inverter application (see Figure 26).

Cross-conduction effect can happen with all types of FET devices while punch-through effect is more related to JFET devices.
Figure 26 shows the cross-conduction and punch-through effects in a power inverter arm delivering positive current to an inductive load. In this case, the AMC feature in the low side driver provides a solution to significantly reduce the risk of cross-conduction/punch-through effects. Similarly, the same effects can be observed at the high side in the case of a power inverter arm delivering negative current.
These 2 effects are due to drain-to-gate coupling through the Miller capacitance of the FETs. They are further enhanced with the gate resistance which is necessary to kill the ringing effect due to parasitic inductances.

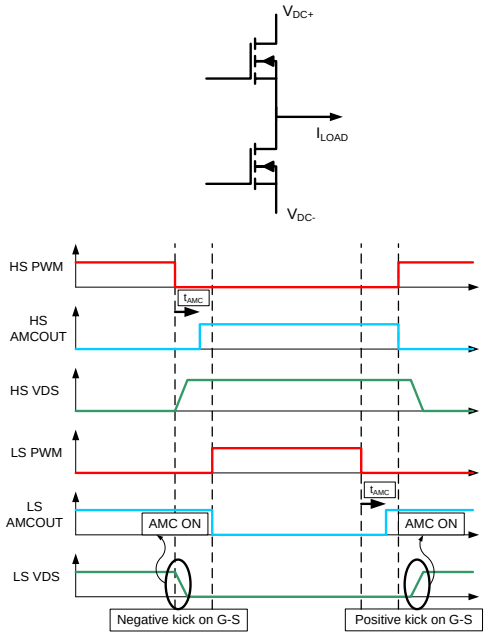


Figure 26. Cross-conduction and punch-through effects in a power inverter arm delivering positive current to an inductive load.

The AMC provides a low impedance path, shunting the gate resistance and so maintains the gate voltage at its desired value (PVSS) (preventing risk of cross-conduction/punch-through).
With HADES2S device, this low-impedance path is implemented with an external transistor controlled by the AMCOUT signal; CHT-NMOS8001 is a suitable and compact transistor to implement this function.
For proper operation, the AMC delay (t_{AMC}) must be carefully adjusted and smaller than the non-overlapping delay between low and high side PWM inputs.
This is made possible thanks to the AMC_D pin which can be connected to an external capacitor.
This t_{AMC} delay is implemented and adjusted by an external capacitor C_{AMC_D} connected to the AMC_D pin and can be calculated as follows:

$$t_{AMC\_D}(ns)=18 * [C_{AMC\_D}\ (pF) + 5.5]$$

Even if the AMC feature is not used in the application, it is mandatory to always put a 7 pF capacitor on AMC_D pin generating a minimum delay of 200 ns.

Output stage

The HADES2S output stage is made of 2 transistors (high-side and low-side) able to deliver current peaks up to 12. Each transistor is driven by a floating internal driver (HSD for High-side, LSD for Low-side). Those drivers are powered by an external capacitor when floating. At the low-side, an internal soft-shutdown transistor (with a typical 33Ω Ron) is connected in parallel with the low-side transistor; it is used in fault situations to gracefully shut down the external power transistor.

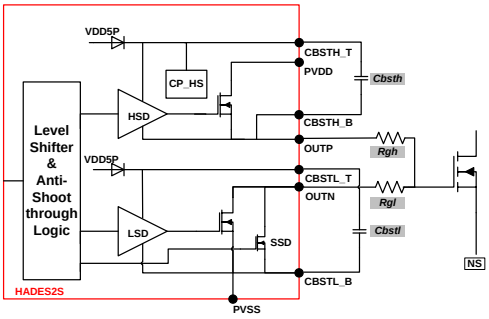


Figure 27 Output stage architecture

Soft-Shutdown

In case of fault detection and if the PWM signal was “high”, the HADES2S push-pull output stage will be turned off in a graceful manner (i.e. by discharging the external power FET gate capacitance with an internal transistor (SSD) having an impedance in the range of 35Ω), this to prevent occurrence of too high dI/dt at power stage level.

Bootstrap output stage

In order to offer best performance in terms of Ron and power device gate current, the high-side transistor is a NMOS device. To drive this transistor, the high-side driver is based on a bootstrap architecture. An external capacitor is needed to feed the high-side driver when ON (indeed, in this case, the driver supply needs to be 5V higher than PVDD).

The low-side driver has also been implemented based on a bootstrap architecture in order to offer best performance in handling push-pull high dI/dt and related effects due to parasitic inductances. In applications where dI/dt is not too high, low-side bootstrap capacitor can be omitted; CBSTL_B should then be connected to PVSS and CBSTL_T to VDD5P.

At start-up, a fault timer (duration: t_{FLT_D}) is started to enable proper charging of the bootstrap capacitors (both high-side and low-side); one needs to ensure that the bootstrap capacitors are properly charged at the end of the fault timer.

Figure 28 provides guidance on fault timer minimum value in function of the bootstrap capacitor value; charging path at start-up includes R_{GH}, R_{GL} and Soft-shutdown transistor Ron.

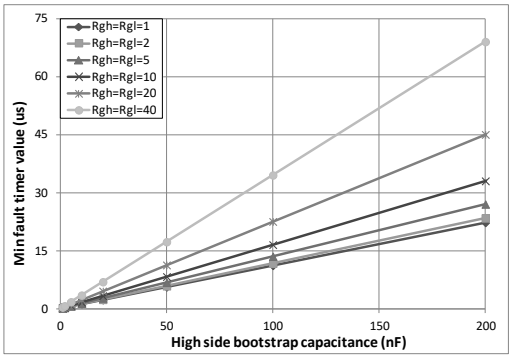


Figure 28

The low-side bootstrap is only used during power supply (PVSS) transient and so needs to be dimensioned to meet criteria below:

$$33\text{nF} < C_{BSTL}(\text{nF}) < 200\ \text{nF}$$

This will ensure that at low-side turn-on, the voltage drop on the bootstrap capacitor is limited to less than 10%.

Thanks to the very low current consumption of the high-side driver and related level shifter and to the charge pump, the high-side bootstrap capacitor dimensioning needs only to ensure that at high-side turn-on, the voltage drop on the bootstrap capacitor is limited to less than 10% (see formula below).

$$33\text{nF} < C_{BSTH}(\text{nF}) < 200\ \text{nF}$$

High-side charge pump (CP_HS)

To support 100% PWM duty cycle, the high-side driver implements an internal charge pump (CP_HS) which function is to maintain the voltage over the Cbsth capacitor. This function does not require any external components nor programming.

Control Interface

Functionally speaking, the control interface is made of 2 signals:

- PWM: input signal controlling the gate driver data path
- FAULT: output signal carrying the fault information from the gate driver function

CMT-HADES2S offers 2 types of control interface:

- Standard 5V digital interface: PWM (input), FAULT (output)
- Modulated control interface enabling transmission over isolation barrier through pulse transformers.

Pin “TRX_MODE” defines mode of operation:

- “0”: Modulated control interface
- “1”: Standard 5V digital interface

In “TRX_MODE=1” mode, PWM input pin implements a Schmitt trigger function on the input to improve noise immunity.

Modulated control interface is fully compatible with HADESV1 chipset and specifically with RHEA device (CHT-TIT4750).

The modulated control interface behaves as follows:

- the transmitter TX-MOD block uses an internally generated clock to modulate the internal fault signal (using OOK modulation scheme) and to generate 2 complementary outputs. The 2 outputs drive the primary side of the pulse transformer in a differential manner.
- The receiver RX-DEMOD block amplifies and demodulates the 2 signals from the transformer secondary side to generate the internal PWM signal.

External pulse transformers are used to transmit the information between primary and secondary. The pulse transformer design has to cope with following constraints:

- Minimize parasitic capacitance (Cp) between Primary and Secondary; ideally Cp should be lower than 0.5 pF to meet 50KV/µs dV/dt robustness)
- Respect isolation requirements
- Primary inductance: 8 µH typ.
- Maximum current on primary side of 20 mA (CMT-HADES2S drive capability)
- Maximum signal frequency: 20 MHz
- Secondary to primary ratio of about 1.1 (ideally 1 but needs to be slightly higher to compensate transformer losses)

Detailed information on the pulse transformer design is available in the EVK-HADES1210 application note.

Routing of the 2 differential signals between CMT-HADES2S and pulse transformer should be as symmetrical as possible. For optimal performance of the PWM isolated link, it might be useful to implement an electrical circuit as described in Figure 29

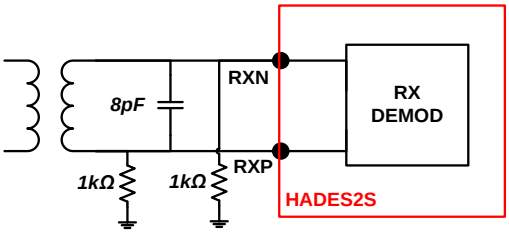


Figure 29

To catch-up all possible faults at board level, TX-MOD is sending “energy” over the transformer when there is no fault at the secondary side; so, any energy loss detection at the primary indicates a fault situation (being at PCB level, in the transformer, at any place in the secondary).

TXP/FAULTB and TXN/FAULT pin behavior is summarized in the table below:

TRX_ MODE	CASE	TXP/ FAULTB	TXN/ FAULT
0	NO FAULT	Energy sent	Energy sent
0	FAULT	No energy sent	No energy sent
0	Start-up	No energy sent	No energy sent
1	NO FAULT	“1”	“0”
1	FAULT	“0”	“1”
1	Start-up	“0”	“0”

Table 1: TXP/TXN pin behavior

Over temperature protection

Die temperature is measured at 3 places:

- close to the high-side output transistor
- close to the low side output transistor
- close to the 5V voltage regulator pass transistor.

If any of those 3 measured temperatures exceeds an internal threshold, TEMP pin will be pulled down.
Temperature threshold can be reached if device is used outside its safe operating area or in case of short-circuit.
If the application would require that in case of over temperature event, a fault is being generated, this function can be implemented by connecting TEMP and UVLO pins together; when TEMP is pulled down, it will generate an UVLO fault by pulling ULVO pin down and so below UVLO low threshold.

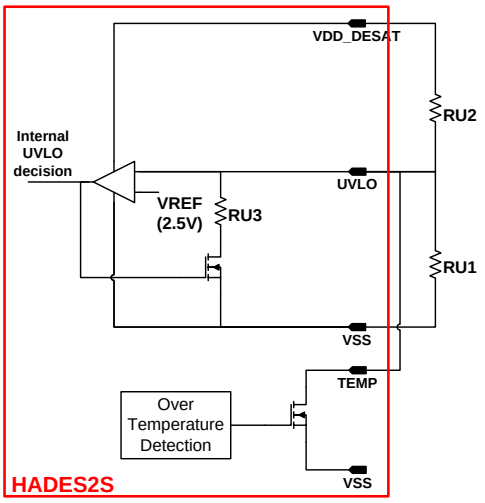


Figure 30: Fault generation by over temperature event

Fault management

In CHT-HADES2S device, fault is generated by any of those situations:

- Power supply is below the UVLO threshold
- Voltage regulator output voltage is below the Power-Good threshold
- Desaturation situation is detected by the DESAT comparator
- Optionally, temperature of the device is above the OTP threshold

Those faults are internally combined to generate an unique fault signal. This signal is latched for a programmable period of time defined by an external capacitor connected to the pin FLT_D.
While the fault is latched, the gate driver is turned off. At the transition between “no fault” and “fault” situation, the gate driver circuit is gracefully shut down.

In case of UVLO fault, after the predefined latch period of time:

- If the fault is still present, the gate driver is kept turned off till the fault disappears
- If the fault disappeared (e.g. temporary UVLO situation), normal operation will resume on the next positive edge of incoming PWM signal

In case of DESAT fault, after the predefined latch period of time:

- the device will go back to normal operation on next positive edge of incoming PWM signal; ie TXN/TXP pins will send OOK modulated signal at timer expiration
- if there was a permanent DESAT fault, on next PWM positive edge (and after DESAT blanking time), a new DESAT fault will be detected and fault timer will be triggered again.

The t_{FLT_D} delay is implemented and adjusted by an external capacitor C_{FLT_D} connected to the FLT_D pin and can be calculated as follows:

$$t_{FLT\_D}\,(\mu s) = 0.5 * C_{FLT\_D}\,(pF)$$

Delay value can range between 10 µs and 500 ms

Device power supplies and decoupling scheme

Figure 31 illustrates the power supplies configuration when driving a SiC MOSFET.

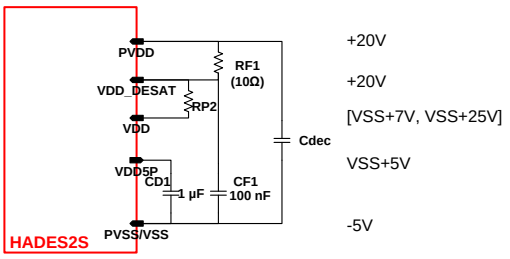


Figure 31. Power supplies configuration (MOSFET case)

RF1 and CF1 implement a mandatory filter to damp the voltage spikes generated by the high speed current variations on PVDD. This filter should have a cut-off frequency set between 1 and 2 MHz; RF1 dimensioning needs to take into account as well the average current flowing through this path. Typical values are: RF1 = 10Ω, CF1 = 100 nF

RP2 resistor can

- either be a “0Ω” resistance in which case, whole voltage drop between VDD_DESAT and “VSS+5V” is managed (wrt to power dissipation) by the internal voltage regulator
- or have a value such that at highest current consumption on VDD5P, VDD stays always higher than “VSS+7V” (for proper operation of the linear voltage regulator); in this case, the power dissipation is spread between RP2 and the internal voltage regulator.

It is also possible to feed VDD from a dedicated power supply (min value of 7V) to minimize power dissipation.

Operation with a single 5V supply is also supported. In this case, VDD and VDD5P must be connected to each other (the internal voltage regulator is short-circuited).

During turn-on/turn-off of the power transistor, large current peaks (sourced from PVDD, sinked into PVSS) will take place.

Decoupling of PVDD and PVSS (Cdec) needs special attention:

- decoupling cap should have a value at least 10 times the equivalent input capacitance of the power device (to limit the voltage drop mainly during turn-on)
- ESR should be in the range of 0.1Ω to also limit voltage drop over the decoupling capacitor
- ESL and parasitic inductance should be minimized (Vdrop = ESL*dI/dt).

Device start-up

Special care has been taken to provide device known behavior during power supply ramp-up.

Figure 22 illustrates a typical start-up sequence; during the start-up phase, the HADES2S device control logic waits that

- VDD_DESAT is above the UVLO threshold
- Voltage regulator output is above Power-Good level.

Once this state is reached, the fault timer is started; during this period, the bootstrap capacitors are charged.
At the end of the timer period, the device enters normal operation; PWM signal propagation starts on next positive edge of the incoming PWM signal.

Table below summarizes the different states in which the device can be and how the device should behave in each of those states

Power Good (VDD5P)	UVLO	Behavior
Not OK	Not OK	OUTP in HiZ, OUTN tied to low level via Soft-Shutdown internal transistor TXN/TXP: "0" Device in "FAULT" state
Not OK	OK	
OK	Not OK	
OK	OK	Normal operation

Table 2: Start-up device behavior

Push-pull stage power dissipation

The power consumption of the push-pull stage (through PVDD) is mainly determined by following external factors:

- Gate charge of the power device (Q)
- Voltage swing on the power device gate (V)
- Switching frequency (Fs).

On top of that, internal device capacitances need also to be charged and discharged.
The power consumption of the output stage is then calculated as follows:

$$P(W)= (1nF*V+Q)*V*Fs$$

The related power dissipation is taking place:

- partly in the push-pull stage (through Ron)
- and partly in the external gate resistors (Rgh, Rgl) (dimensioned and used to control the switching speed)

As a rule of thumb, split between push-pull and external gate resistors is according to following formula:

$$Ravg = (Rgh+Rgl)/2$$
$$Ppush\text{-}pull[W] = P*1/(1+Ravg)$$
$$Prgate[W] = P*Ravg/(1+Ravg)$$

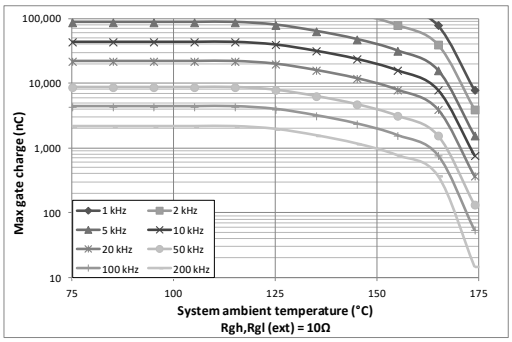
Safe Operating Area

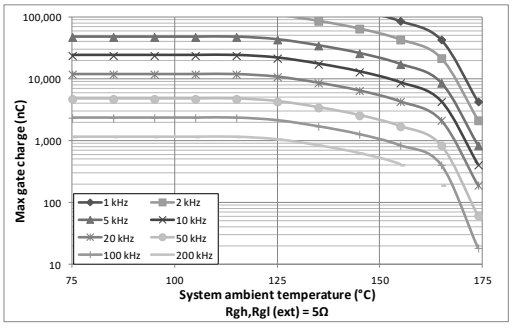
The HADES2S device power dissipation is largely dependent on the switching frequency and the gate charge of the power device it drives.

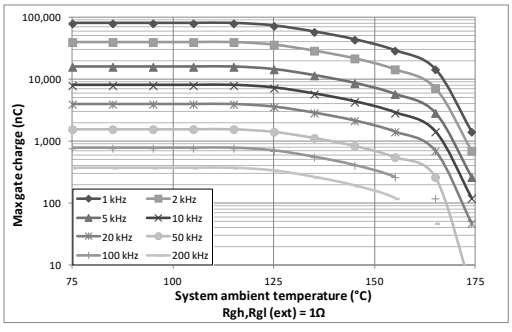
System designers also need to maintain HADES2S device within safe operating zone wrt to:

- junction temperature (max 175°C)
- max power dissipation (1W)
- max push-pull average current (1.5A).

To help system designers matching system requirements with HADES2S safe operating zone, the graphs below provide guidance about supported gate charge in function of system ambient temperature (still air), PWM switching frequency and external gate resistance (power device gate voltage swing = 25V; junction-2-air thermal resistance in still air = 55°C/W).







Current consumption

Formulas below provide guidance on the current consumption of the HADES2S device; this information shall be mainly used to dimension the power supplies.

In fault state,

- I_{VDD_DESAT}= 0.9mA
- I_{VDD} = 1.8mA
- I_{PVDD} = 0mA

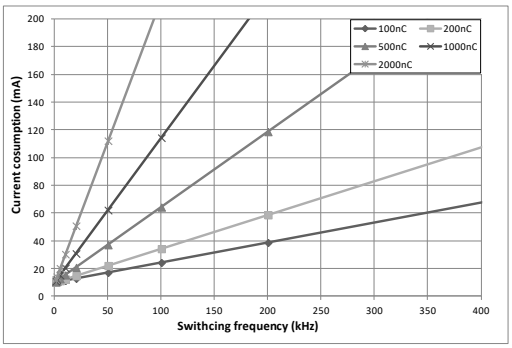
In normal operation,

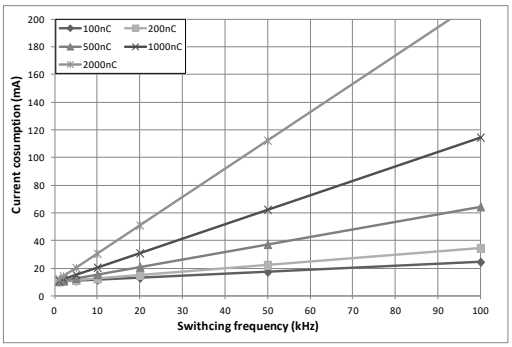
- I_{VDD_DESAT}= 0.9mA
- I_{VDD} = 9.2mA + 1000*(19e^{-09}*Fs) mA
- I_{PVDD} = 1000*(1e^{-09}*V_{PVDD}+Qe)*Fs mA

Where:

- Qe: external gate charge (in C)
- Fs: Switching frequency (in Hz)
- V_{PVDD}: “PVDD-PVSS” voltage (in Volt)

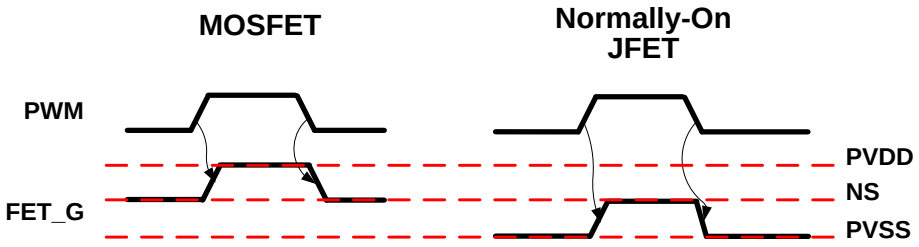
The following graph provides information on total device current consumption (normal operation) in function of PWM switching frequency (PVDD=25V).





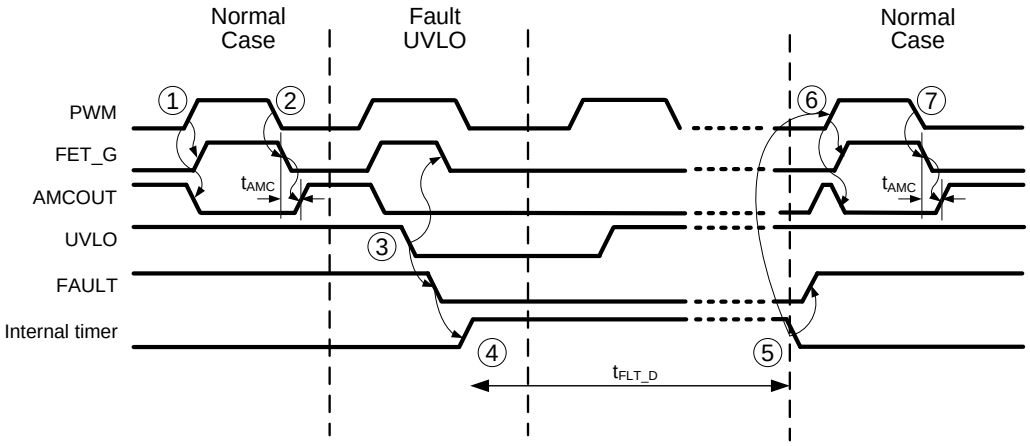
Timing diagrams

Normal case (MOSFET/Normally-On)



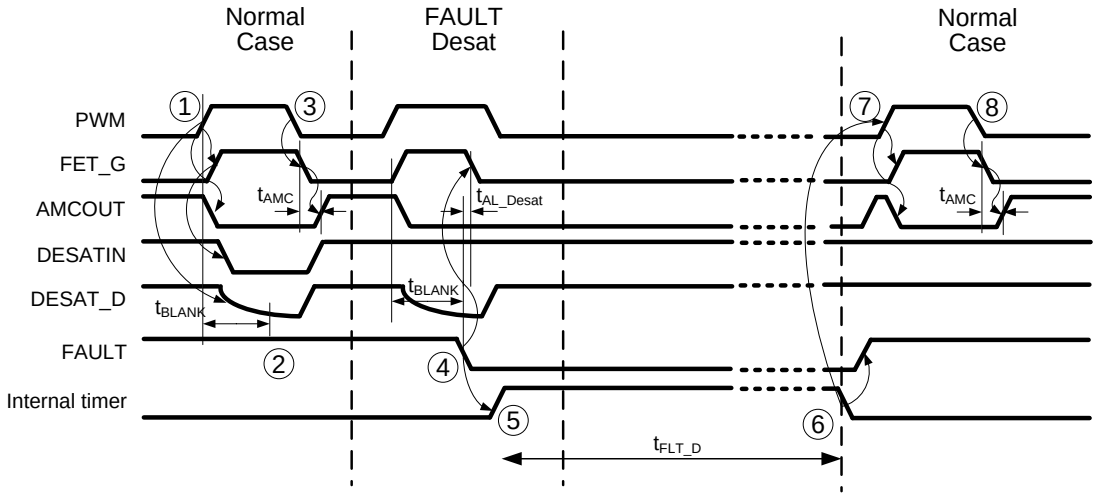
FET type	Description
MOSFET	PWM =HIGH: MOSFET gate is charged to PVDD power supply: PWM = LOW: MOSFET gate is discharged to PVSS power supply. MOSFET source is connected to NS (VSS is negative wrt to NS)
Normally-On JFET	PWM =HIGH: JFET gate is charged to NS power supply: PWM = LOW: JFET gate is discharged to PVSS power supply. JFET source is connected to NS

Fault event: UVLO



Main events	Description
①	On the rising edge of PWM input signal, the signal OUTP is driven high to turn on the FET. At the same time, the signal AMCOUT is turned off to disable the Active Miller Clamp external transistor
②	On the falling edge of PWM input signal, the signal OUTN is driven low to turn off the FET. After t_{AMC} delay, the signal AMCOUT is driven high to turn on the Active Miller Clamp external transistor
③	Undervoltage is detected by the UVLO circuitry and an internal UVLO error is generated. This error resets the FAULT signal and activates the internal fault timer.
④	The internal fault timer lasts t_{FLT_D} seconds; during that period, PWM input signal is blanked and FET is turned off by means of OUTN signal.
⑤	At the end of fault timer period, the logic is going back to normal operation. If the fault is still present, the device remains in fault state till the fault 21disappears. If the fault is no more present, normal circuit operation is resumed.
⑥	On the rising edge of PWM input signal, the signal OUTP is driven high to turn on the FET. At the same time, the signal AMCOUT is turned off to disable the Active Miller Clamp external transistor.
⑦	On the falling edge of PWM input signal, the signal OUTN is driven low to turn off the FET. After t_{AMC} delay, the signal AMCOUT is driven high to turn on the Active Miller Clamp external transistor.

Fault event: Desaturation



Main events	Description
①	On the rising edge of PWM input signal, the signal OUTP is driven high to turn on the FET. At the same time, the signal AMCOUT is turned off to disable the Active Miller Clamp external transistor
②	Since DESATIN signal was below DESAT_T threshold after t_{BLANK} time, no DESAT error is detected and normal operation continues
③	On the falling edge of PWM input signal, the signal OUTN is driven low to turn off the FET. After t_{AMC} delay, the signal AMCOUT is driven high to turn on the Active Miller Clamp external transistor
④	Desaturation error is detected since DESATIN signal was above DESAT_T threshold after t_{BLANK} time. This error resets the FAULT signal and activates the internal fault timer.
⑤	The internal fault timer lasts t_{FLT_D} seconds; during that period, PWM input signal is blanked and FET is turned off by means of OUTN signal.
⑥	At the end of fault timer period, the logic is going back to normal operation. If the fault is still present, timer is restarted for a new period. If the fault is no more present, normal circuit operation is resumed.
⑦	On the rising edge of PWM input signal, the signal OUTP is driven high to turn on the FET. At the same time, the signal AMCOUT is turned off to disable the Active Miller Clamp external transistor.
⑧	On the falling edge of PWM input signal, the signal OUTN is driven low to turn off the FET. After t_{AMC} delay, the signal AMCOUT is driven high to turn on the Active Miller Clamp external transistor.

Application Diagrams

Driving a SiC MOSFET

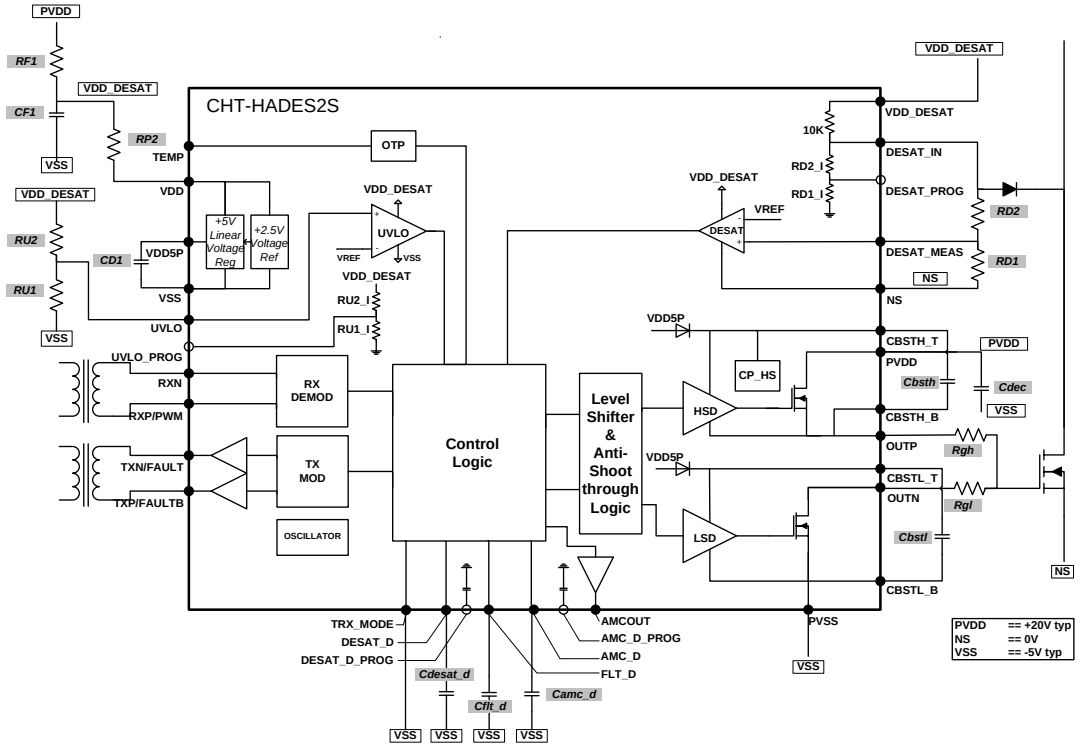


Figure 32: Typical application schematic (SiC MOSFET power device)

The SiC MOSJFET is turned on once a positive swing (wrt to the MOSFET source; typically 20V for best performance) is applied to the gate. To turn the MOSFET off, it is recommended to apply a negative (wrt to MOSFET source; typically -2 to -5V) voltage on the gate.

The position of VDD_DESAT and VSS with respect to NS is set by a midpoint generated by the external power supply which has to be connected to NS.

Local decoupling between PVDD and PVSS (Cdec) is mandatory as large current peaks flow through those supply connections during gate switching. The decoupling capacitor must deliver the total power MOSFET gate charge with minimum supply voltage loss.

The high-side (pin OUTP) and low-side (pin OUTN) drivers inside CMT-HADESV2 pull the MOSFET gate voltage up and down.

Resistor (Rgh, Rgl) on OUTP/OUTN limits the gate current at turn-on/turn-off; those resistors control as well the switching time of the MOSFET and therefore the dV/dt in order to reduce probability of shoot-through current (parasitic turn-on of the blocking device in a half-bridge configuration). They also help damping oscillations and limiting voltage overshoot at the MOSFET gate which could result from stray inductances in the gate drive circuit and which could cause damage to the devices. Typical values range from 1 to 20 ohms, depending on the power FET size.

At positive switching, the bootstrap capacitor (connected between CBSTH_T and CBSTH_B) biases the high-side drivers above the positive supply voltage VDD. The typical bootstrap capacitor value is 33nF. After the transition, the internal charge-pumps keep the high-side drivers on till the next negative transition without any minimum switching frequency constraint. The low-side driver is also floating and uses a bootstrap capacitor; this is required for applications where very high dI/dt takes place on the gate loop (which induces internally to HADES2S large swing on PVSS node).

If the Active Miller Clamp function is used, following a turn off of the power device, AMCOUT signal will become high after a defined time by the capacitor connected to the pin AMC_D

The HADES2S voltage regulator input supply (VDD) can be connected:

- either directly to VDD_DESAT (highest power supply); in this case, all regulator losses are concentrated in HADES2S device
- or to VDD_DESAT via an external resistor in order to distribute the losses between the resistor and HADES2S
- or to an additional power supply (e.g. 7V above PVSS)

Following parameters can be programmed through external resistors:

- DESAT threshold
- UVLO threshold

Following parameters can be programmed through external capacitors:

- DESAT blanking time
- Active Miller Clamp delay
- Fault latching time

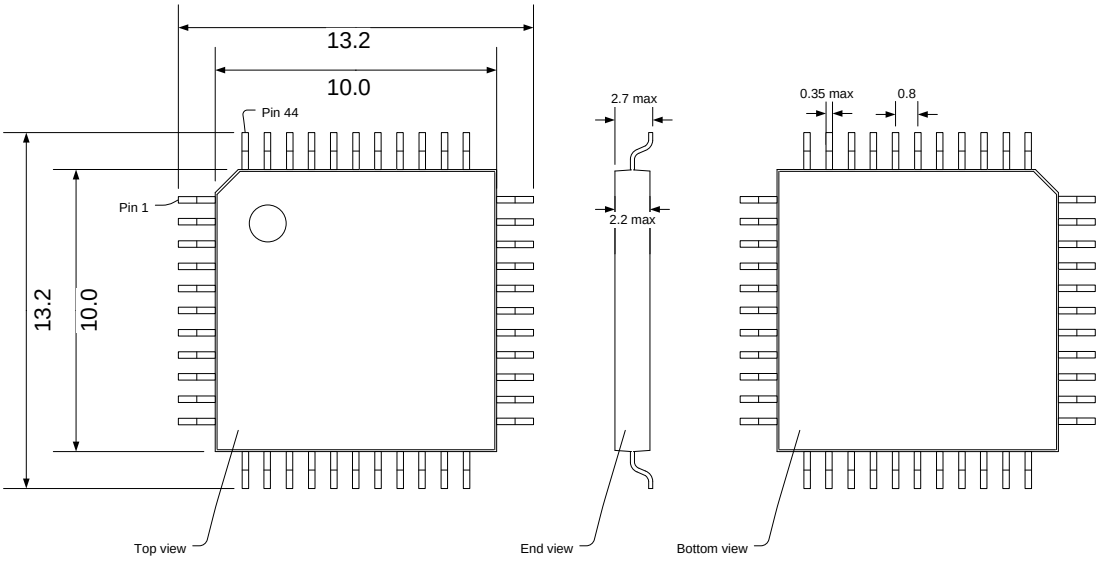
Application Diagrams (cnt'd)

Driving a SiC MOSFET

Table below lists all required passive devices in the typical application drawn in Figure 32 and provides guidance on typical value and important selection criteria for those passives.

Passive ID	Type	Function	Typ. value	Operational voltage range	Comment
Rgh	R	High-side gate resistor	[1-20]Ω		Pay attention to power dissipation when selecting component
Rgl	R	Low-side gate resistor	[1-20]Ω		Pay attention to power dissipation when selecting component
Cbsth	C	High-side bootstrap capacitor	[33-200]nF	5V	
Cbstl	C	Low-side bootstrap capacitor	[33-200]nF	5V	
Cdec	C	Local decoupling between PVDD and PVSS	100 nF	30V	Pay attention to the ESR and ESL of this capacitor since it needs to handle large dI/dt
RF1	R	Spike filtering	[1-20]Ω		
CF1	C	Decoupling and filter capacitor	100 nF	30V	
RP2	R	Optional resistor to spread dissipation between HADES2S and RP2	[0-1]KΩ		Pay attention to power dissipation when selecting component
CD1	C	Voltage regulator output capacitor	1µF	5V	ESR typ. : 100mΩ
Camc_d	C	AMC delay setting	20 pF	5V	== 300 ns AMC delay
Cflt_d	C	Fault timer value setting	Depends on system design	5V	
Cdesat_d	C	Desat blanking delays setting		5V	
RU1	R	UVLO threshold setting			
RU2	R	UVLO threshold setting			
RD1	R	Desat threshold setting			
RD2	R	Desat threshold setting			

Package Drawing



PQFP44 physical dimensions in mm (tolerance : +/- 0.2 mm)

Ordering Information

Product Name	Ordering Reference	Package	Marking
CMT-HADES2S	CMT-TIT0521C-PQFP44-T	PQFP44	CMT-TIT0521C

Contact & Ordering

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