



**General Description**

- AlphaSGT™ N-Channel Power MOSFET
- Combination of Low  $R_{DS(ON)}$  and wide safe operating area (SOA)
- Higher in-rush current enabled for faster start-up and shorter down time
- PB-free lead plating, RoHS complaint, Halogen-free
- Top Side cooling for improved thermal performance

**Applications**

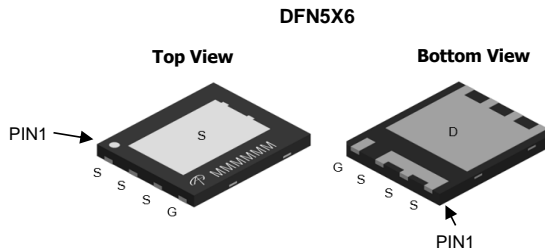
- Telecom
- Solar
- DC-DC

**Product Summary**

$V_{DS}$	100V
$I_D$ (at $V_{GS}=10V$ )	197A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 3.4mΩ
$R_{DS(ON)}$ (at $V_{GS}=6V$ )	< 4.6mΩ

100% UIS Tested  
100% Rg Tested

Max  $T_j=175^{\circ}C$



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONA66916	DFN 5x6	Tape & Reel	5000

**Absolute Maximum Ratings  $T_A=25^{\circ}C$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^{\circ}C$	197
		$T_C=100^{\circ}C$	139
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	330	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^{\circ}C$	30
		$T_A=70^{\circ}C$	25
Avalanche Current <sup>C</sup>	$I_{AS}$	60	A
Avalanche energy L=0.1mH <sup>C</sup>	$E_{AS}$	180	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^{\circ}C$	300
		$T_C=100^{\circ}C$	150
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^{\circ}C$	7.5
		$T_A=70^{\circ}C$	5.2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^{\circ}C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	15	20	$^{\circ}C/W$
Maximum Junction-to-Ambient <sup>A D</sup>				
Maximum Junction-to-Ambient <sup>A D</sup>	$R_{\theta JC}$	0.3	0.55	$^{\circ}C/W$
Maximum Junction-to-Case, bottom				
Maximum Junction-to-Case, top	$R_{\theta JC}$	0.25	0.5	$^{\circ}C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.4	3	3.6	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		2.8 5	3.4 6	mΩ
		V <sub>GS</sub> =6V, I <sub>D</sub> =20A		3.7	4.6	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		75		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				197	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz		5300		pF
C <sub>oss</sub>	Output Capacitance			1500		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			26		pF
R <sub>g</sub>	Gate resistance	f=1MHz	0.8	1.6	2.4	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =20A		66	95	nC
Q <sub>gs</sub>	Gate Source Charge			18		nC
Q <sub>gd</sub>	Gate Drain Charge			12		nC
Q <sub>oss</sub>	Output Charge	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V		123		nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		15		ns
t <sub>r</sub>	Turn-On Rise Time			8		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			46.5		ns
t <sub>f</sub>	Turn-Off Fall Time			13		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, di/dt=500A/μs		43		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, di/dt=500A/μs		280		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25° C. The Power dissipation P<sub>D(SM)</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=175° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

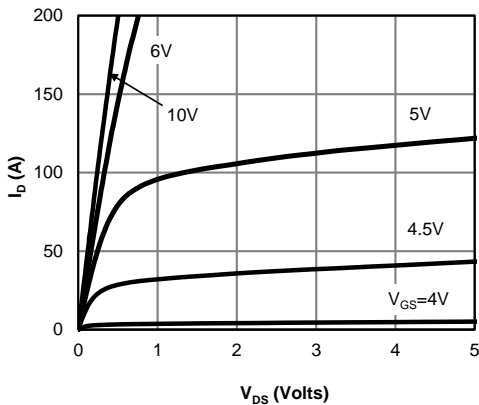
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175° C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

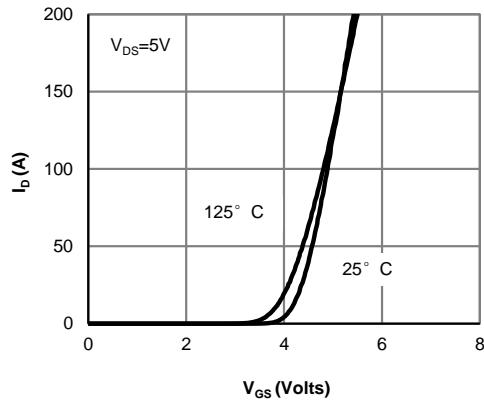
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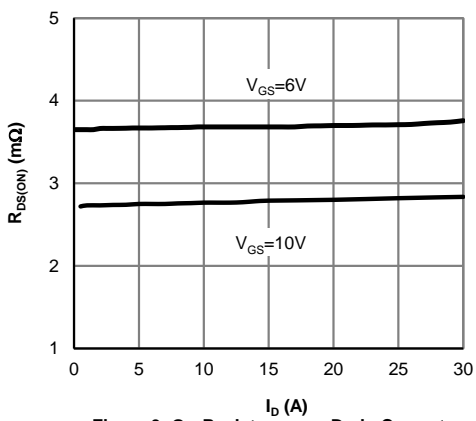
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



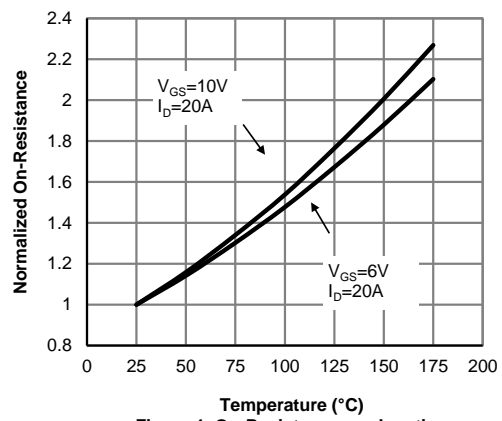
**Figure 1: On-Region Characteristics (Note E)**



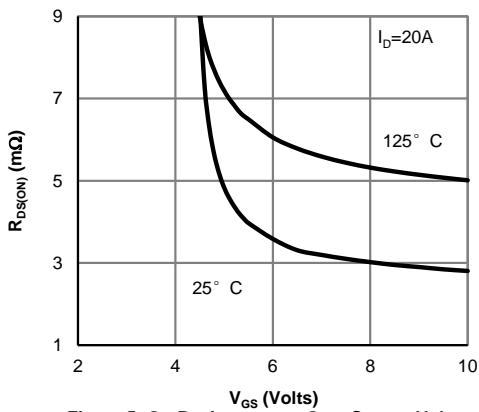
**Figure 2: Transfer Characteristics (Note E)**



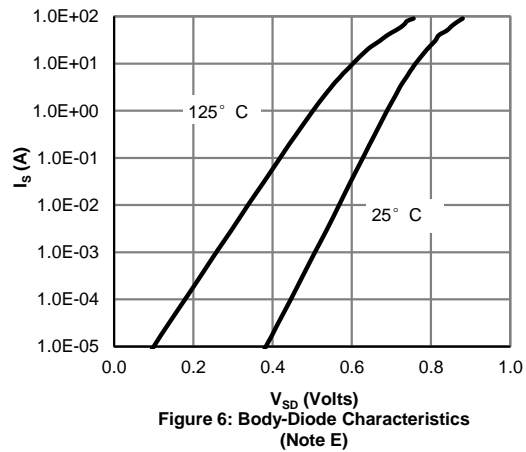
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

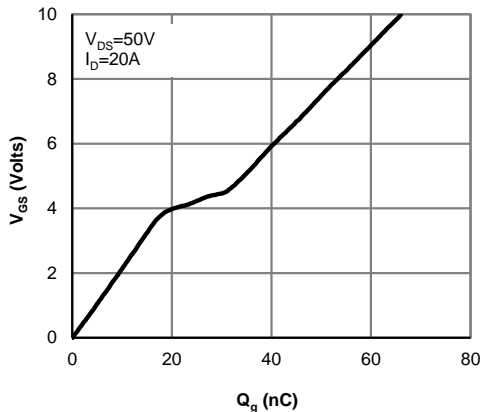


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

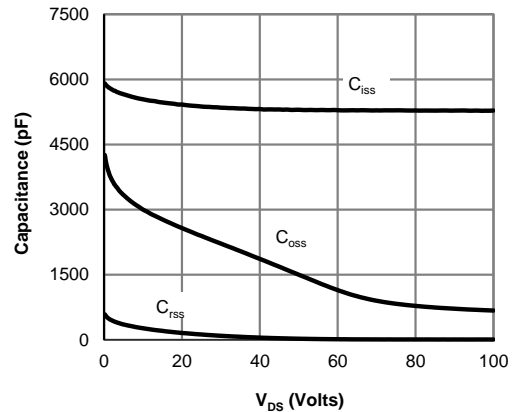


**Figure 6: Body-Diode Characteristics (Note E)**

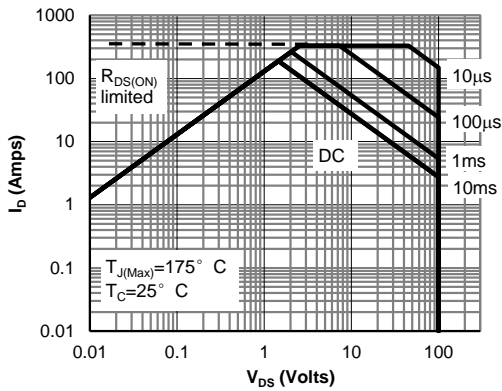
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



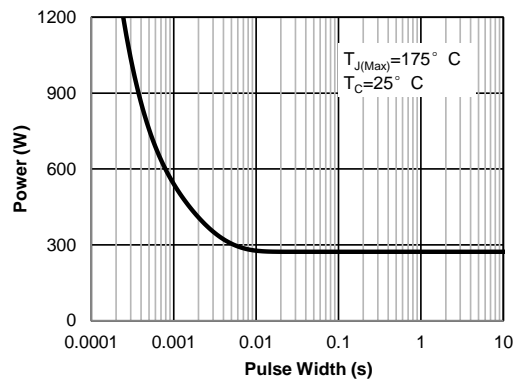
**Figure 7: Gate-Charge Characteristics**



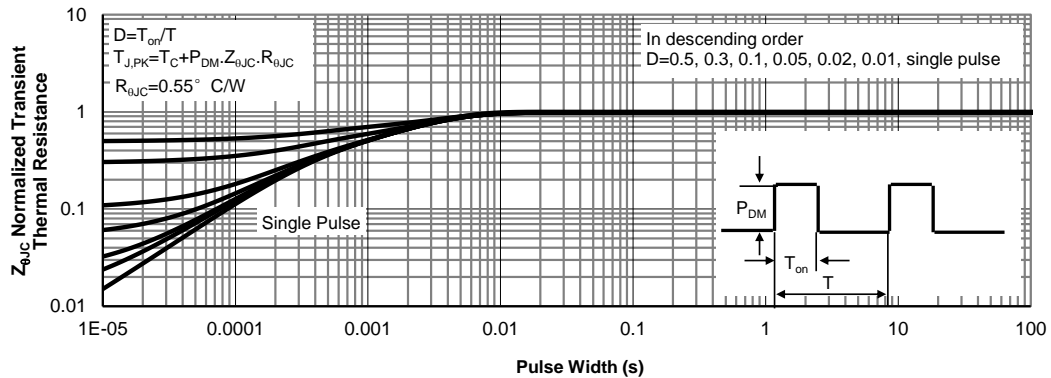
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case-Bottom (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance-Bottom (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

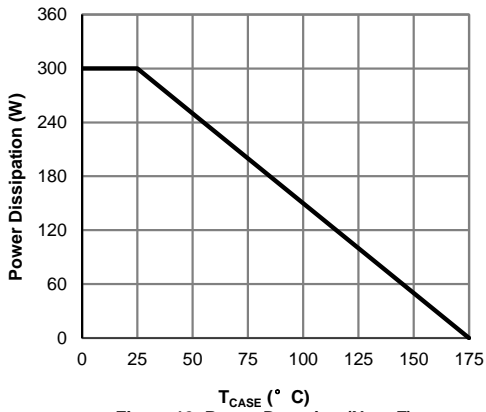


Figure 12: Power De-rating (Note F)

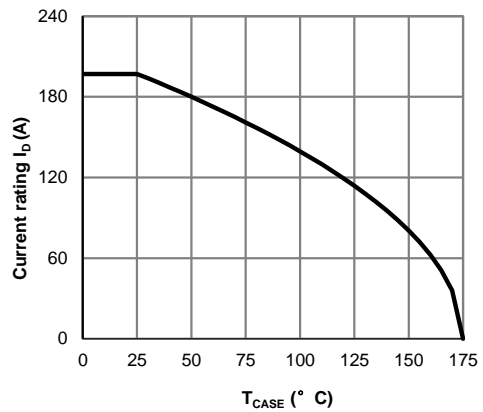


Figure 13: Current De-rating (Note F)

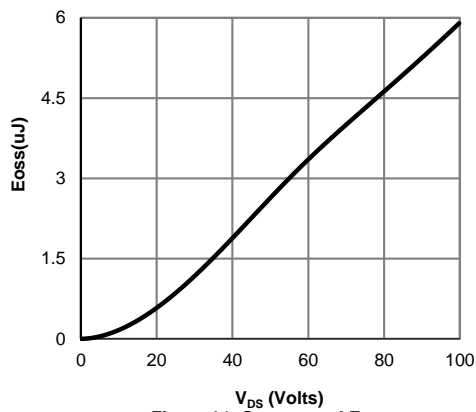


Figure 14: Coss stored Energy

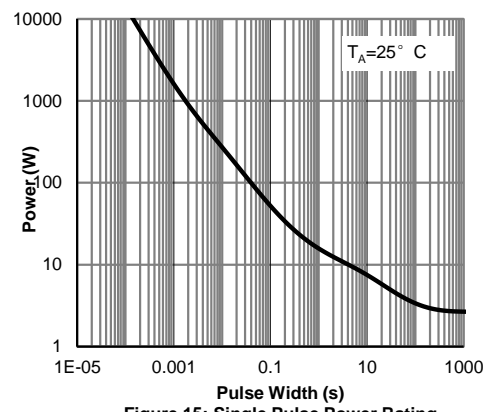


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

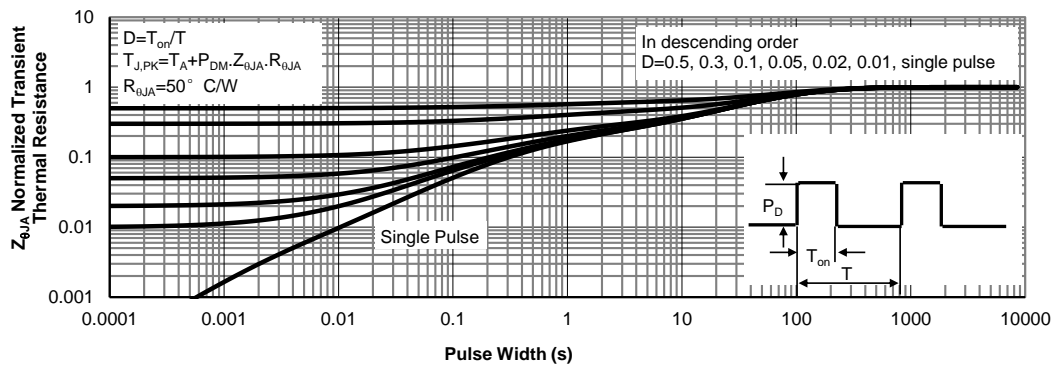
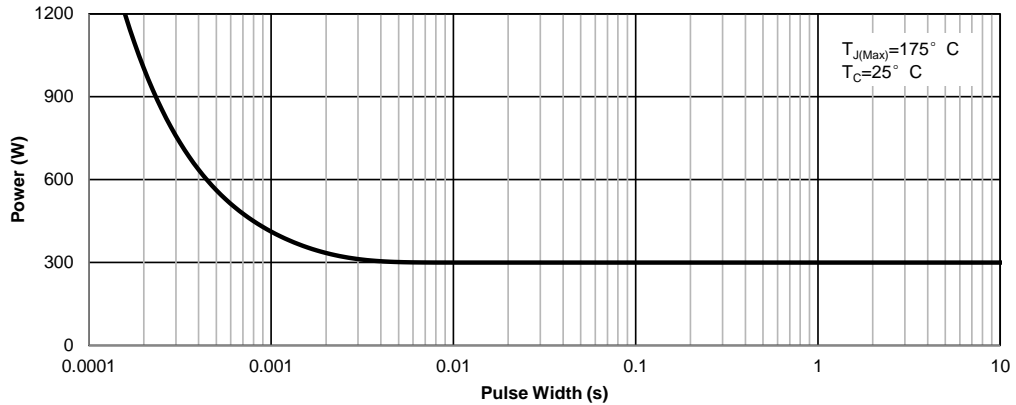
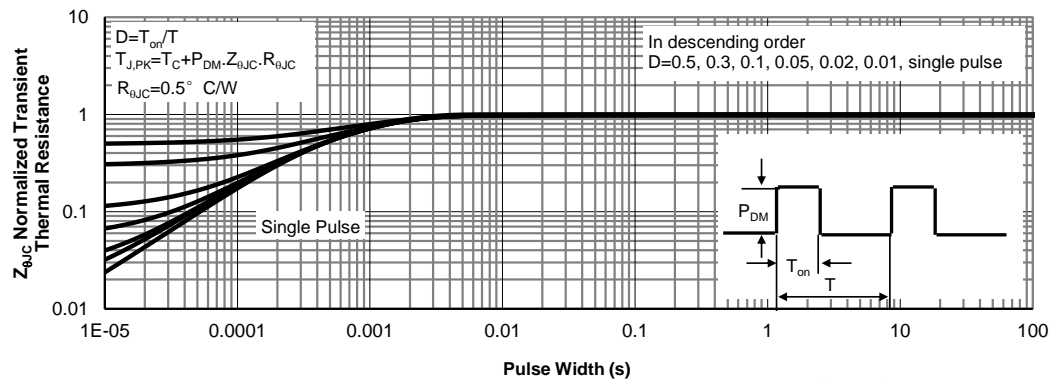


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



**Figure 17: Single Pulse Power Rating Junction-to-Case-Top (Note F)**



**Figure 18: Normalized Maximum Transient Thermal Impedance-Top (Note F)**

Figure A: Gate Charge Test Circuit & Waveforms

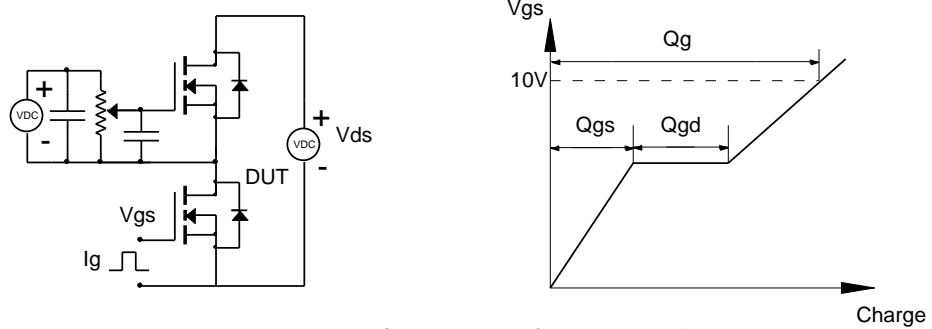


Figure B: Resistive Switching Test Circuit & Waveforms

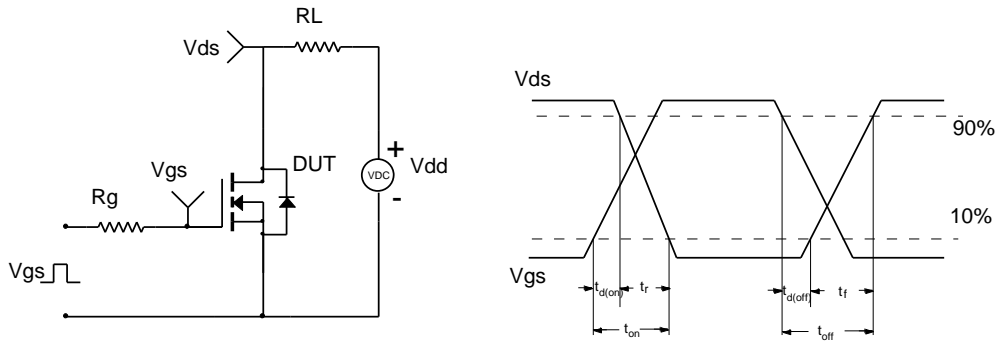


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

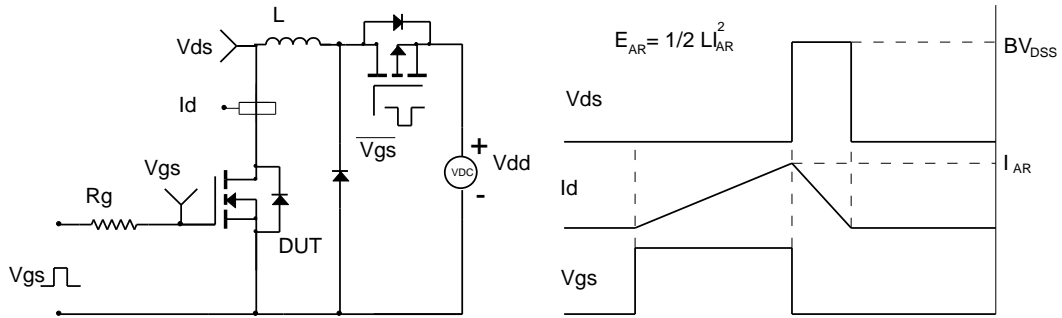


Figure D: Diode Recovery Test Circuit & Waveforms

