

## DATASHEET

# UHB100SC12E1BC3N

## 1200V-100A SiC Half-Bridge Module

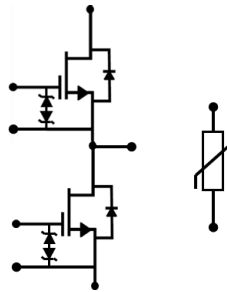
Rev. B, February 2024

### Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's silicon-like gate-drive characteristics allows the use of unipolar gate drives, compatible with Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the E1B module package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive. Advanced Ag sintering die attach technology gives the module superior thermal performance.

### Features

- ◆ On-resistance:  $R_{DS(on)} = 9.4m\Omega$  (typ)
- ◆ Operating temperature: 150°C (max)
- ◆ Excellent reverse recovery:  $Q_{rr} = 1000nC$
- ◆ Low body diode voltage:  $V_{FSD} = 1.4V$
- ◆ Low gate charge:  $Q_G = 170nC$
- ◆ Threshold voltage  $V_{G(th)}$ : 5V (typ) allowing 0 to 15V drive
- ◆ Low intrinsic capacitance
- ◆ ESD protected: HBM class 2 and CDM class C3



Part Number	Package	Marking
UHB100SC12E1BC3N	E1B	UHB100SC12E1BC3N

### Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating



## Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	$V_{DS}$		1200	V
Gate-source voltage	$V_{GS}$	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current <sup>1</sup>	$I_D$	$T_C < 85^\circ\text{C}$	100	A
Pulsed drain current <sup>2</sup>	$I_{DM}$	$T_C = 25^\circ\text{C}$	700	A
Power dissipation per switch	$P_{tot}$	$T_C = 25^\circ\text{C}$	417	W
Maximum junction temperature	$T_{J,max}$		150	$^\circ\text{C}$
Operating and storage temperature	$T_J, T_{STG}$		-55 to 150	$^\circ\text{C}$

1. Limited by package lead count

2. Pulse width  $t_p$  limited by  $T_{J,max}$

## Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case per switch	$R_{\theta JC}$			0.23	0.3	$^\circ\text{C/W}$

## NTC Thermistor Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Rated resistance	$R_{25}$	$T_{NTC} = 25^\circ\text{C}$		5		k $\Omega$
Resistance value tolerance	$\Delta R/R$	$T_{NTC} = 25^\circ\text{C}$	-5		5	%
Power dissipation	$P_{25}$	$T_{NTC} = 25^\circ\text{C}$			20	mW
B constant	$B_{25/50}$	$R_2 = R_{25} \exp [B_{25/50} (1/T_2 - 1/(298.15 \text{ K}))]$		3375		K

## Module

Parameter	Symbol	Test Conditions	Value	Units
Isolation voltage	$V_{ISOL}$	RMS, f = 50 Hz, t = 1 min	3	kV
Internal isolation			$\text{Al}_2\text{O}_3$	
Creepage distance		Terminal to heatsink	11.5	mm
		Terminal to terminal	6.3	
Clearance distance		Terminal to heatsink	10	mm
		Terminal to terminal	5	
Stray inductance module	$L_{SCE}$		11	nH

## SiC FET Electrical Characteristics ( $T_J = +25^\circ\text{C}$ unless otherwise specified)

### Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	$BV_{DS}$	$V_{GS}=0V, I_D=8mA$	1200			V
Total drain leakage current	$I_{DSS}$	$V_{DS}=1200V,$ $V_{GS}=0V, T_J=25^\circ\text{C}$		32	600	$\mu\text{A}$
		$V_{DS}=1200V,$ $V_{GS}=0V, T_J=150^\circ\text{C}$		100		
Total gate leakage current	$I_{GSS}$	$V_{DS}=0V, T_J=25^\circ\text{C},$ $V_{GS}=-20V / +20V$		24	80	$\mu\text{A}$
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=70A,$ $T_J=25^\circ\text{C}$		9.4	12	m $\Omega$
		$V_{GS}=12V, I_D=70A,$ $T_J=125^\circ\text{C}$		15		
		$V_{GS}=12V, I_D=70A,$ $T_J=150^\circ\text{C}$		17.5		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=40mA$	4	5	6	V
Gate resistance	$R_G$	$f=1\text{MHz}, \text{open drain}$		1.1		$\Omega$

### Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current <sup>1</sup>	$I_S$	$T_C < 85^\circ\text{C}$			100	A
Diode pulse current <sup>2</sup>	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			700	A
Forward voltage	$V_{FSD}$	$V_{GS}=0V, I_S=70A,$ $T_J=25^\circ\text{C}$		1.4	2	V
		$V_{GS}=0V, I_S=70A,$ $T_J=150^\circ\text{C}$		1.63		
Reverse recovery charge	$Q_{rr}$	$V_{DS}=800V, I_S=100A,$ $V_{GS}=-5V, R_G=5\Omega$		1000		nC
Reverse recovery time	$t_{rr}$	$di/dt=4100A/\mu\text{s},$ $T_J=25^\circ\text{C}$		41		ns
Reverse recovery charge	$Q_{rr}$	$V_{DS}=800V, I_S=100A,$ $V_{GS}=-5V, R_G=5\Omega$		920		nC
Reverse recovery time	$t_{rr}$	$di/dt=4100A/\mu\text{s},$ $T_J=150^\circ\text{C}$		40		ns

## Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units	
			Min	Typ	Max		
Input capacitance	$C_{iss}$	$V_{DS}=800V, V_{GS}=0V$ $f=100kHz$		5859		pF	
Output capacitance	$C_{oss}$			372			
Reverse transfer capacitance	$C_{rss}$			6.7			
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		480		pF	
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		1065		pF	
$C_{OSS}$ stored energy	$E_{oss}$	$V_{DS}=800V, V_{GS}=0V$		154		$\mu J$	
Total gate charge	$Q_G$	$V_{DS}=800V, I_D=100A,$ $V_{GS} = -5V$ to 15V		170		nC	
Gate-drain charge	$Q_{GD}$			38			
Gate-source charge	$Q_{GS}$			62			
Turn-on delay time	$t_{d(on)}$	Notes 3 and 4 $V_{DS}=800V, I_D=100A,$ Gate Driver = -5V to +15V, $R_{G\_EXT}=5\Omega,$ Inductive Load, FWD: $V_{GS} = -5V,$ $R_{G\_EXT} = 5\Omega, T_J=25^\circ C$		50		ns	
Rise time	$t_r$			33			
Turn-off delay time	$t_{d(off)}$			65			
Fall time	$t_f$			12			
Turn-on energy	$E_{ON}$			1442			$\mu J$
Turn-off energy	$E_{OFF}$			308			
Total switching energy	$E_{TOTAL}$		1750				
Turn-on delay time	$t_{d(on)}$	Notes 3 and 4 $V_{DS}=800V, I_D=100A,$ Gate Driver = -5V to +15V, $R_{G\_EXT}=5\Omega,$ Inductive Load, FWD: $V_{GS} = -5V,$ $R_{G\_EXT} = 5\Omega, T_J=150^\circ C$		45		ns	
Rise time	$t_r$			31			
Turn-off delay time	$t_{d(off)}$			70			
Fall time	$t_f$			11			
Turn-on energy	$E_{ON}$			1280			$\mu J$
Turn-off energy	$E_{OFF}$			266			
Total switching energy	$E_{TOTAL}$		1546				

3. Measured with the half-bridge mode switching test circuit in Figure 23.

4. A bus RC snubber ( $R_{BS} = 2.5\Omega, C_{BS}=200nF$ ) must be applied to reduce the power loop high frequency oscillations.

### Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units		
			Min	Typ	Max			
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=800V$ , $I_D=100A$ , Gate Driver = -5V to +15V, $R_{G,EXT} = 1\Omega$ , inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 1\Omega$ , RC snubber: $R_S=5\Omega$ and $C_S=440pF$ , $T_J=25^\circ C$		27.2		ns		
Rise time	$t_r$			18.4				
Turn-off delay time	$t_{d(off)}$			57.6				
Fall time	$t_f$			16				
Turn-on energy including $R_S$ energy	$E_{ON}$		Notes 5 and 6, $V_{DS}=800V$ , $I_D=100A$ , Gate Driver = -5V to +15V, $R_{G,EXT} = 1\Omega$ , inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 1\Omega$ , RC snubber: $R_S=5\Omega$ and $C_S=440pF$ , $T_J=150^\circ C$		510		$\mu J$	
Turn-off energy including $R_S$ energy	$E_{OFF}$				518			
Total switching energy	$E_{TOTAL}$				1028			
Snubber $R_S$ energy during turn-on	$E_{RS\_ON}$				30			
Snubber $R_S$ energy during turn-off	$E_{RS\_OFF}$			28				
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=800V$ , $I_D=100A$ , Gate Driver = -5V to +15V, $R_{G,EXT} = 1\Omega$ , inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 1\Omega$ , RC snubber: $R_S=5\Omega$ and $C_S=440pF$ , $T_J=150^\circ C$			28			ns
Rise time	$t_r$				13.6			
Turn-off delay time	$t_{d(off)}$				61.6			
Fall time	$t_f$			18.4				
Turn-on energy including $R_S$ energy	$E_{ON}$		Notes 5 and 6, $V_{DS}=800V$ , $I_D=100A$ , Gate Driver = -5V to +15V, $R_{G,EXT} = 1\Omega$ , inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 1\Omega$ , RC snubber: $R_S=5\Omega$ and $C_S=440pF$ , $T_J=150^\circ C$		382		$\mu J$	
Turn-off energy including $R_S$ energy	$E_{OFF}$				521			
Total switching energy	$E_{TOTAL}$				903			
Snubber $R_S$ energy during turn-on	$E_{RS\_ON}$				30			
Snubber $R_S$ energy during turn-off	$E_{RS\_OFF}$			25				

5. Measured with the switching test circuit in Figure 24.

6. In this table, the switching energies (turn-on energy, turn-off energy and total energy) presented include the device RC snubber energy losses.

## SiC FET Typical Performance Diagrams

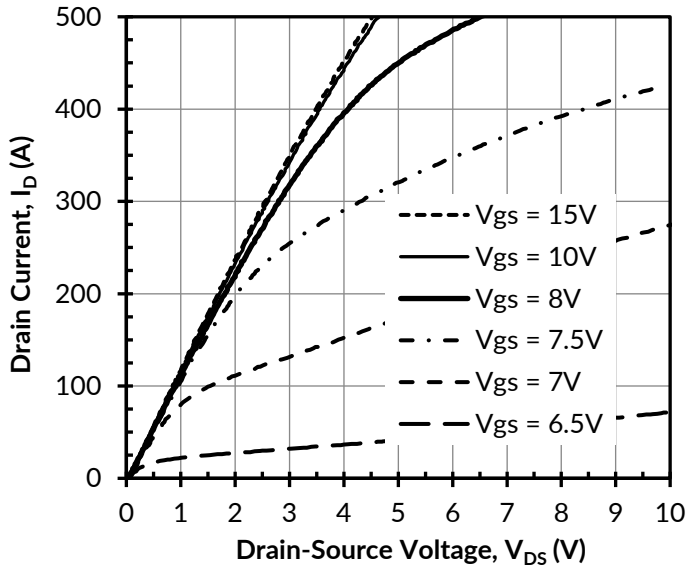


Figure 1. Typical output characteristics at  $T_j = -55^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

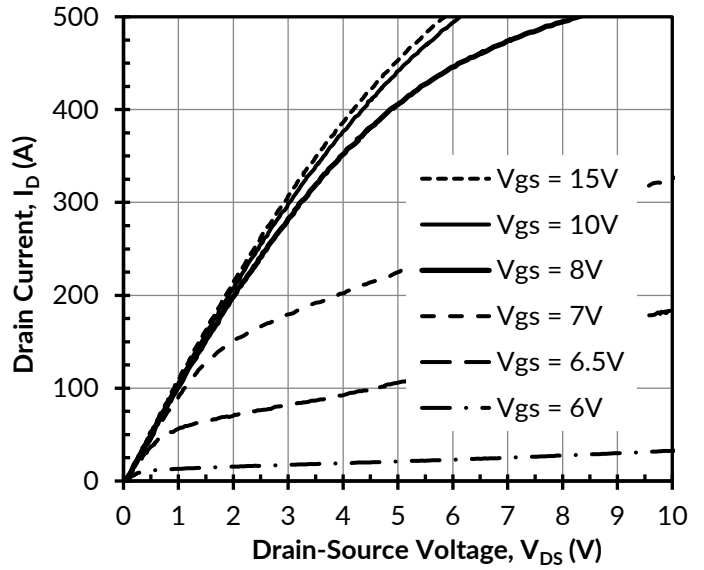


Figure 2. Typical output characteristics at  $T_j = 25^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

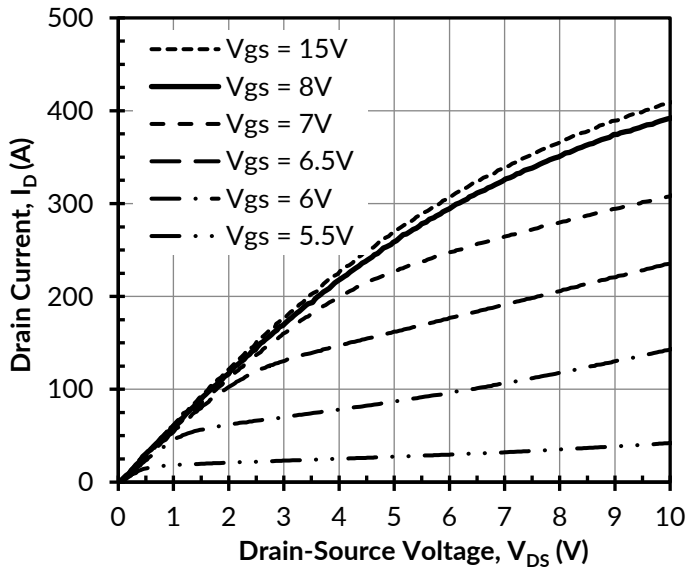


Figure 3. Typical output characteristics at  $T_j = 150^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

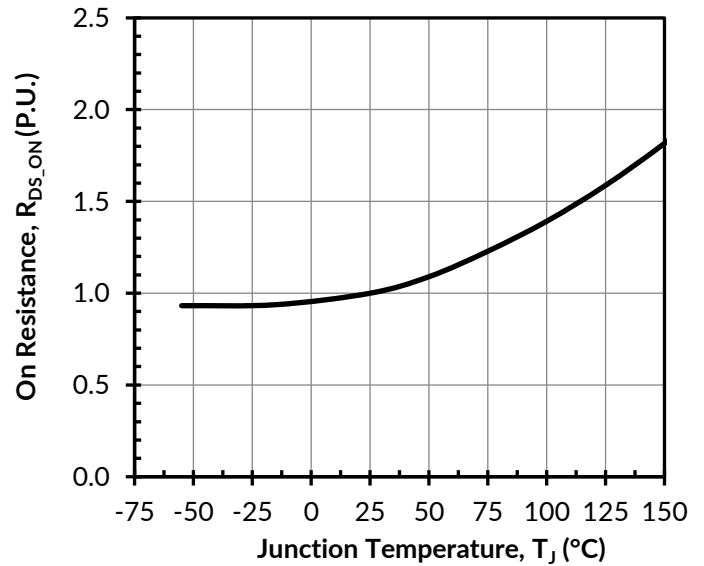


Figure 4. Normalized on-resistance vs. temperature at  $V_{GS} = 12\text{V}$  and  $I_D = 70\text{A}$

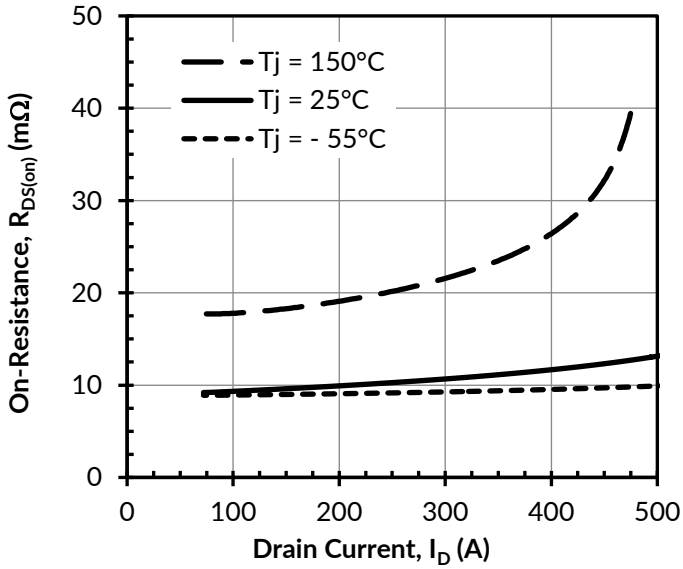


Figure 5. Typical drain-source on-resistances at  $V_{GS} = 12\text{V}$

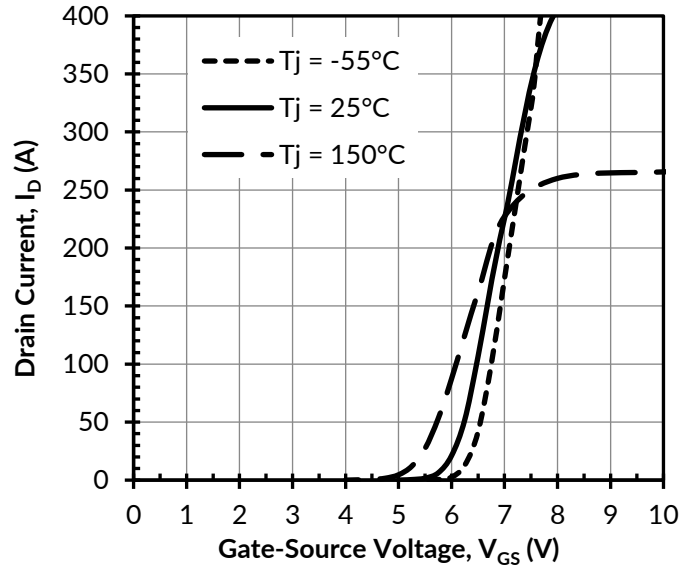


Figure 6. Typical transfer characteristics at  $V_{DS} = 5\text{V}$

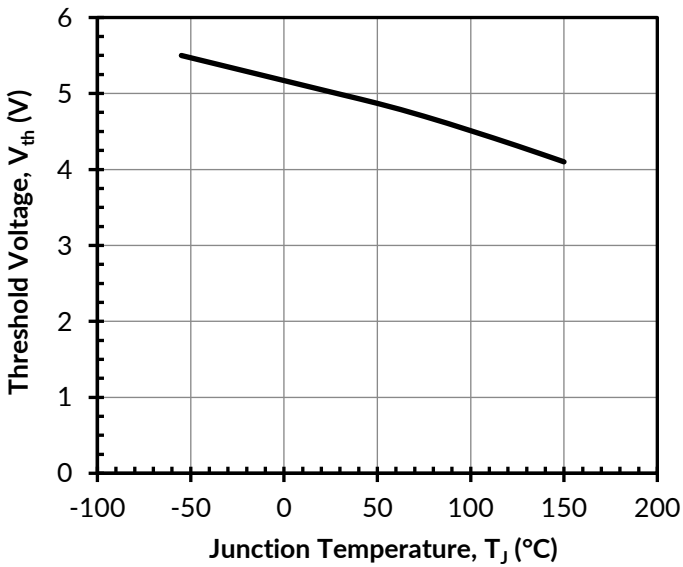


Figure 7. Threshold voltage vs. junction temperature at  $V_{DS} = 5\text{V}$  and  $I_D = 40\text{mA}$

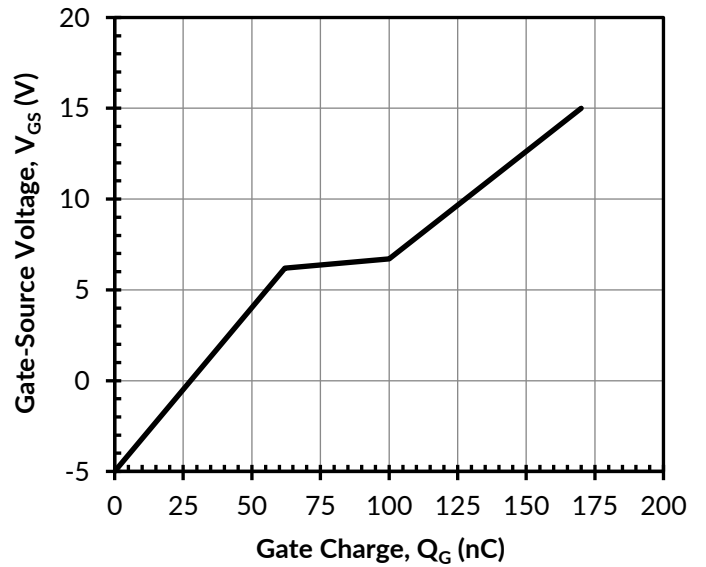


Figure 8. Typical gate charge at  $V_{DS} = 800\text{V}$  and  $I_D = 100\text{A}$

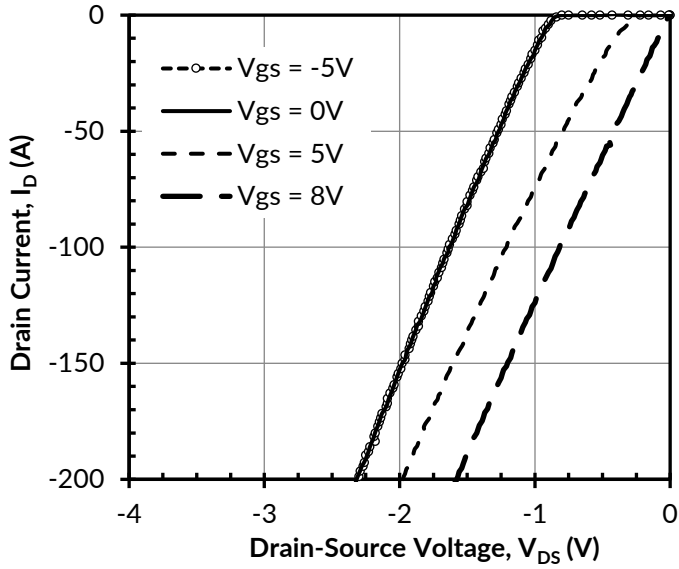


Figure 9. 3rd quadrant characteristics at  $T_j = -55^\circ\text{C}$

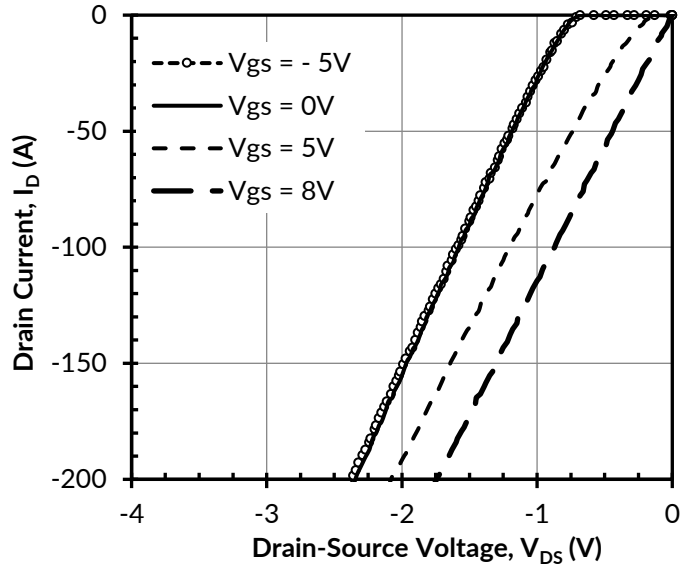


Figure 10. 3rd quadrant characteristics at  $T_j = 25^\circ\text{C}$

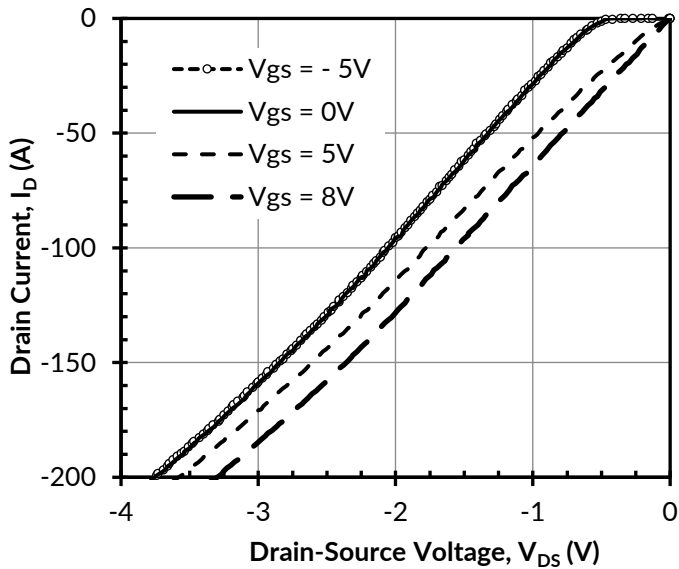


Figure 11. 3rd quadrant characteristics at  $T_j = 150^\circ\text{C}$

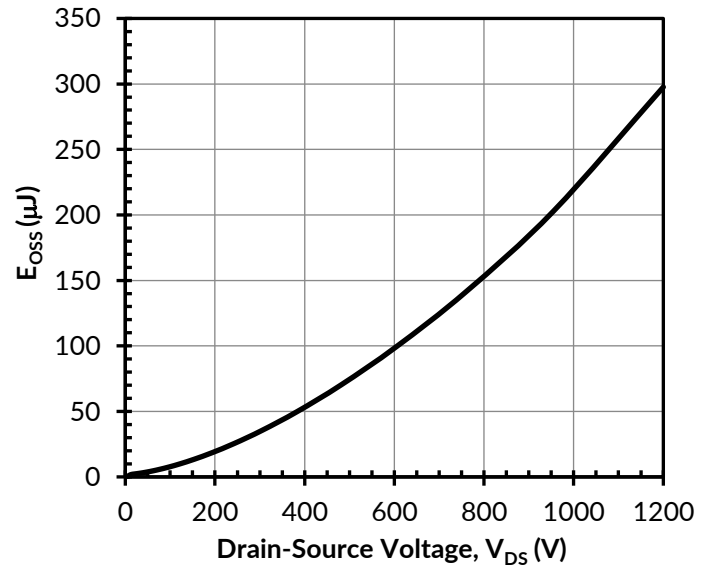


Figure 12. Typical stored energy in  $C_{OSS}$  at  $V_{GS} = 0\text{V}$



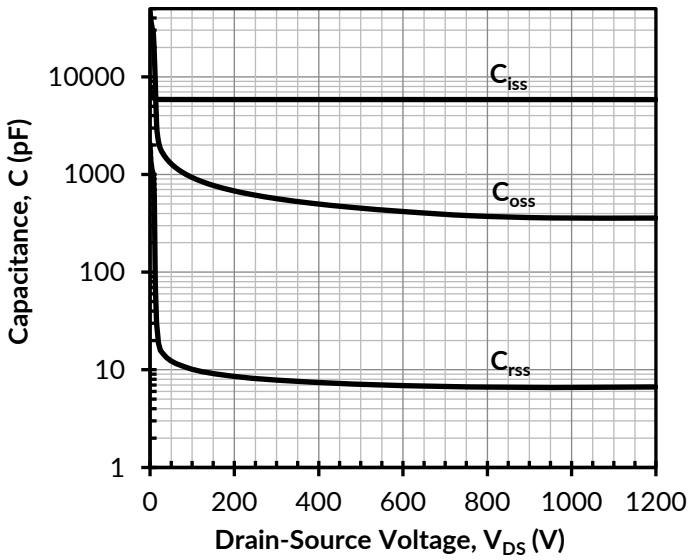


Figure 13. Typical capacitances at  $f = 100\text{kHz}$  and  $V_{GS} = 0\text{V}$

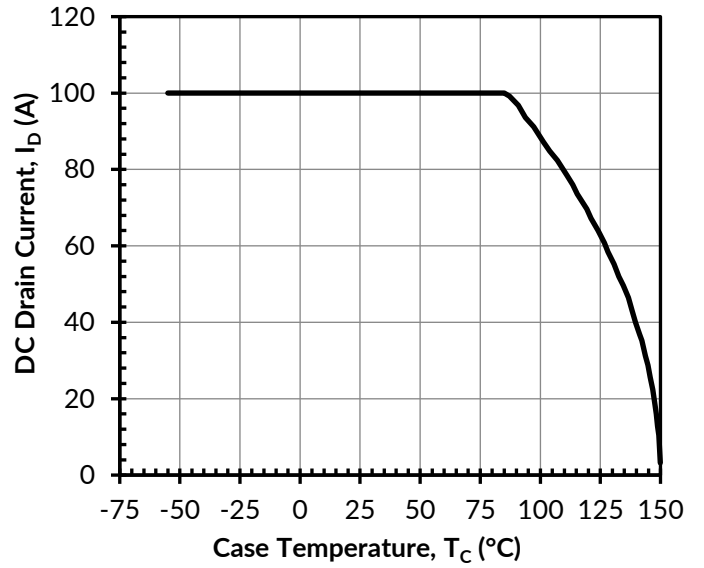


Figure 14. DC drain current derating

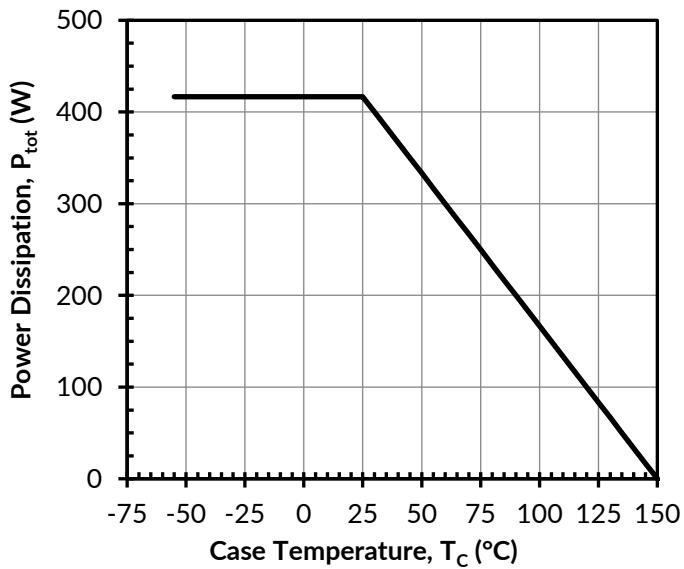


Figure 15. Total power dissipation

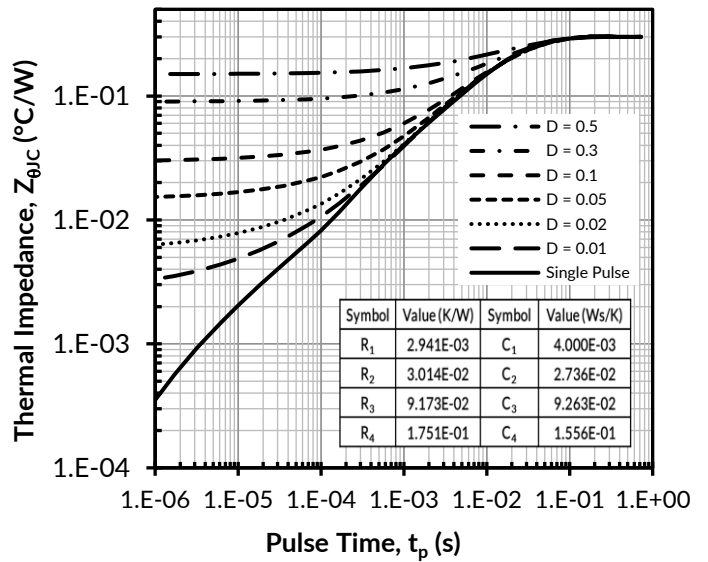


Figure 16. Maximum transient thermal impedance and parameters for thermal equivalent circuit (Foster) model

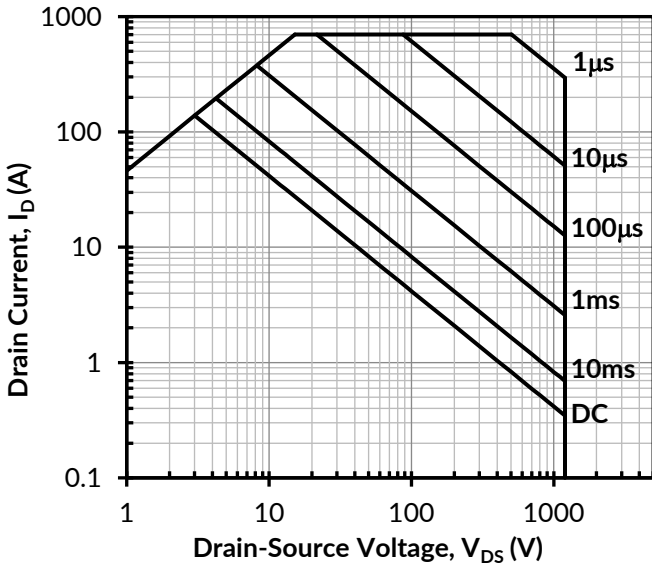


Figure 17. Safe operation area at  $T_C = 25^\circ\text{C}$ ,  $D = 0$ , Parameter  $t_p$

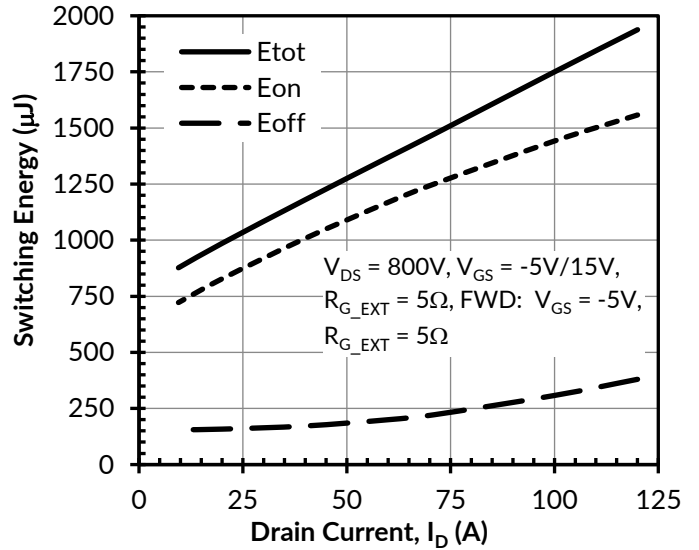


Figure 18. Clamped inductive switching energy vs. drain current at  $T_J = 25^\circ\text{C}$

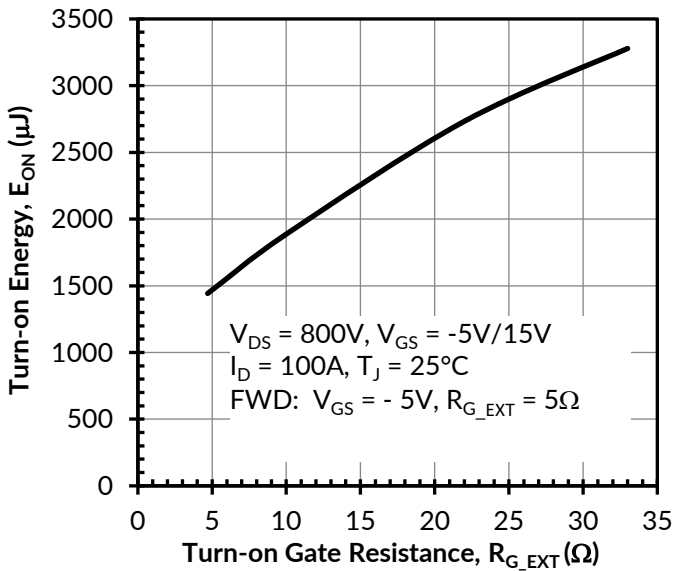


Figure 19. Clamped inductive switching turn-on energy vs. turn-on gate resistance  $R_G$

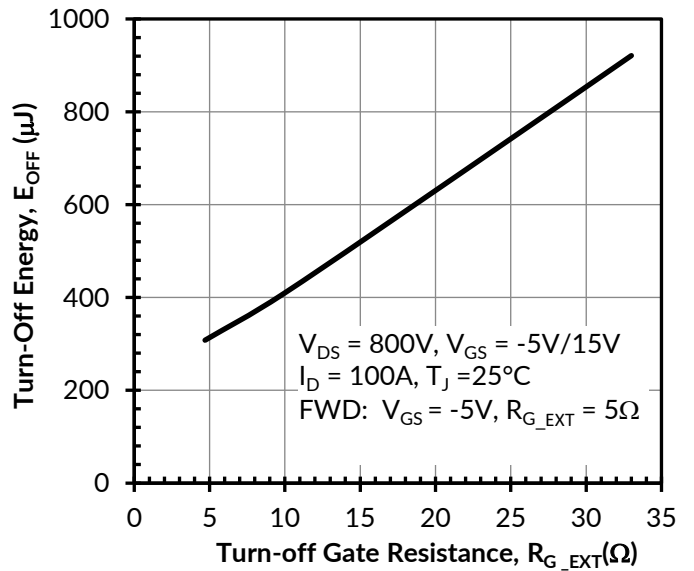


Figure 20. Clamped inductive switching turn-off energy vs. turn-off gate resistance  $R_G$

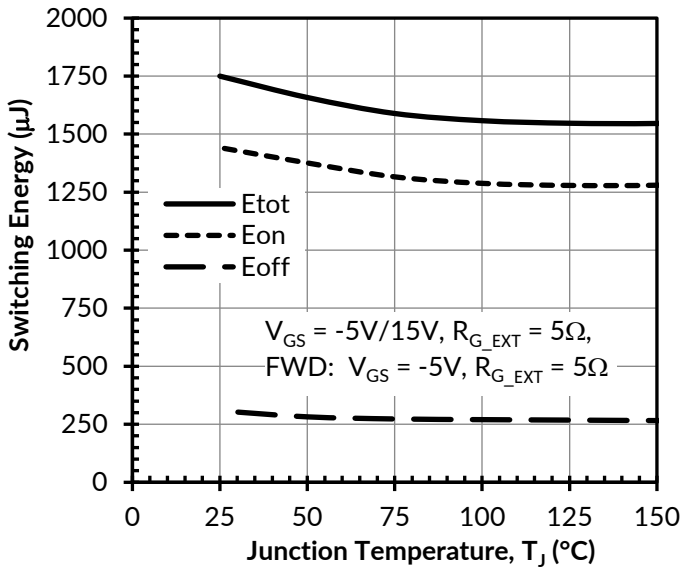


Figure 21. Clamped inductive switching energy vs. junction temperature at  $V_{DS} = 800V$  and  $I_D = 100A$

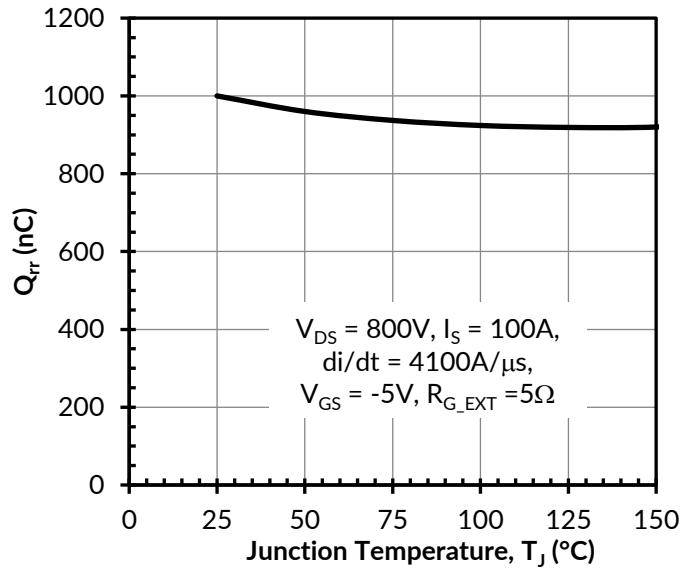


Figure 22. Reverse recovery charge  $Q_{rr}$  vs. junction temperature

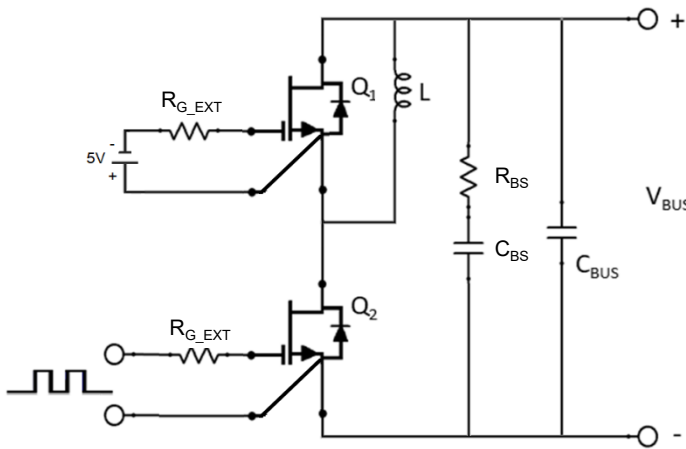


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ( $R_{BS} = 2.5\Omega$ ,  $C_{BS}=200nF$ ) must be applied to reduce the power loop high frequency oscillations.

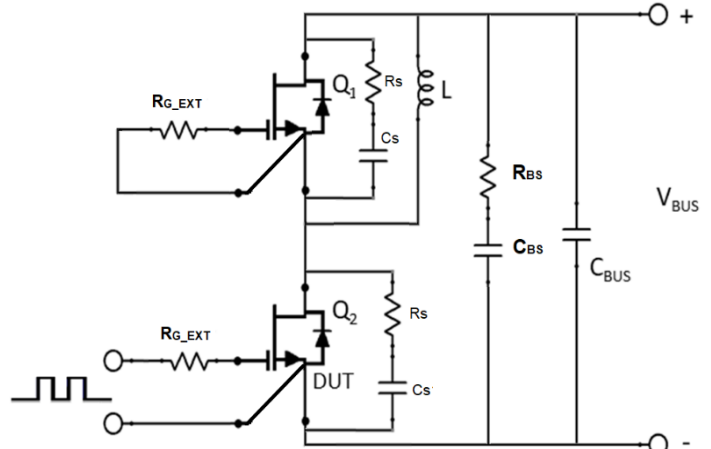
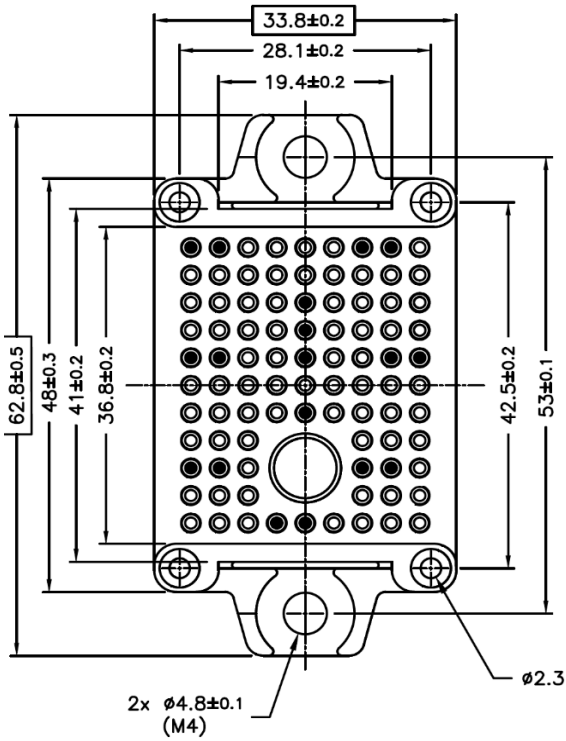
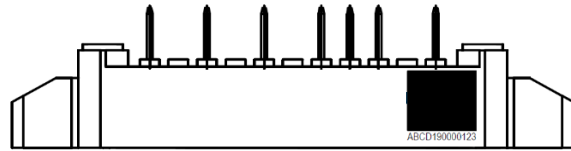
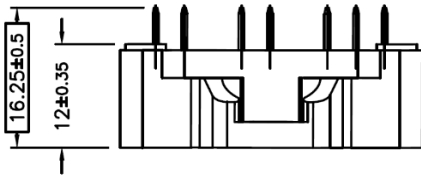
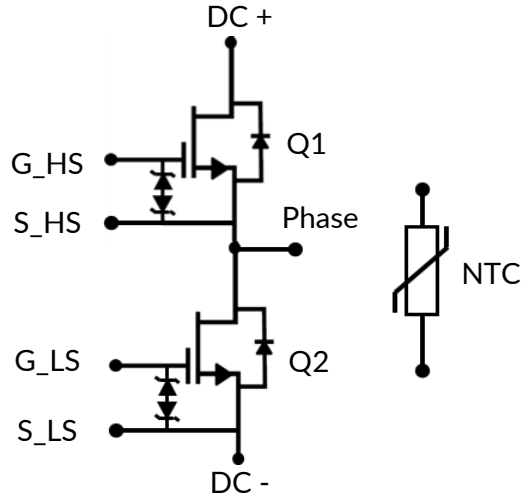
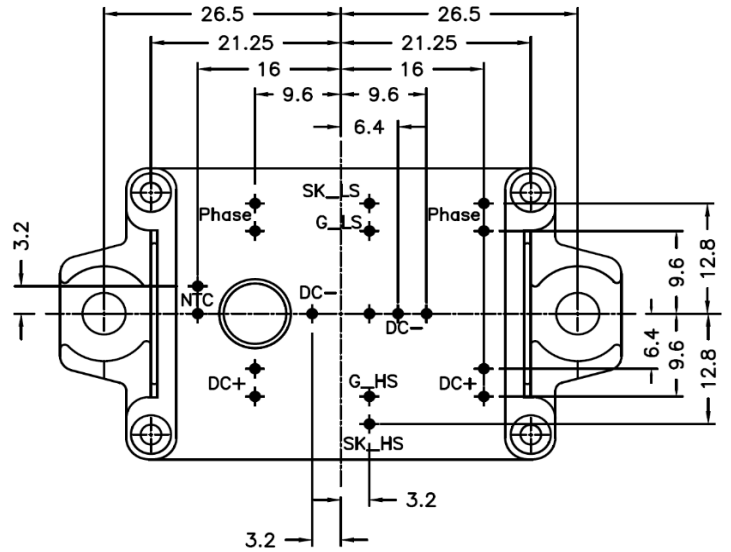


Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers ( $R_s = 5\Omega$ ,  $C_s = 440pF$ ) and a bus RC snubber ( $R_{BS} = 2.5\Omega$ ,  $C_{BS}=200nF$ ).

Circuit Diagram and Pin Definitions



PCB HOLE PATTERN



NOTES:

1. All dimensions in millimeters (mm)
2. General tolerance:  $\pm 0.1\text{mm}$ , unless otherwise specified

## Important Mounting Information

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

## Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see <https://www.qorvo.com/design-hub>.

A snubber circuit with a small  $R_{(G)}$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_{(G)}$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_{(G)}$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_{(G)}$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the Qorvo website at <https://www.qorvo.com/design-hub>.

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