EPC7009L16SH
## Radiation-Hardened GaN Gate Driver Datasheet

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Features

- Compatible with all EPC Space Discrete eGaN® products
- Single GAN Gate Driver Integrated Circuit
- Independent Pull-Up and Pull-Down gate drive outputs
- Capable of Driving 5000 pF+ Loads
- High Speed Capability: 3.0 MHz+
- 3 V Logic-Compatible Input control
- Non-Inverting and Inverting Logic Inputs
- 10 V Supply for Interface to Legacy PWM Controllers
- Hermetic Ceramic QLCC SMT Package
- Extremely Small Size: 0.228 x 0.183 x 0.085 inches
- Guaranteed Total Ionizing Dose:
  - Rated to 1000 krad(Si) for HDR (50-300 rad(Si)/s
  - Rated to 100 krad(Si) for LDR (100 mrads(Si)/s
- Single Event:
  - SEE immunity for LET of 84 MeV/mg/cm^2
- Neutron Fluence:
  - Maintains Specification up to 1×10^{15} N/cm^2

Applications

- DC-DC conversion
- Satellite Electrical
- Power Switches/Actuators
- Motor Drivers
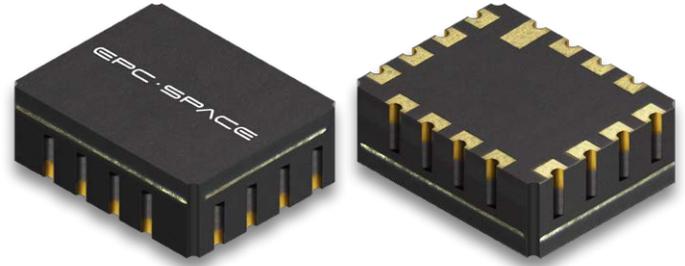
EPC7009L16SH

Radiation-Hardened Single Output GaN Gate Driver Monolithic IC

Description

The EPC7009L16SH is a radiation hardened, high-speed gate-driver, implemented as an integrated circuit (IC) using EPC's proprietary eGaN® technology. The EPC7009 GaN IC contains an on-chip 10 V to 5.25 V linear regulator, under-voltage lockout protection and independent pull-up and pull-down outputs to both optimize and simplify the gate-drive to an external GaN FET. The IC is packaged in an innovative, space-saving hermetic 16-pin SMT package.

Typical Application Circuit

Non-Inverting Mode Low-Side eGaN® HEMT Gate Driver

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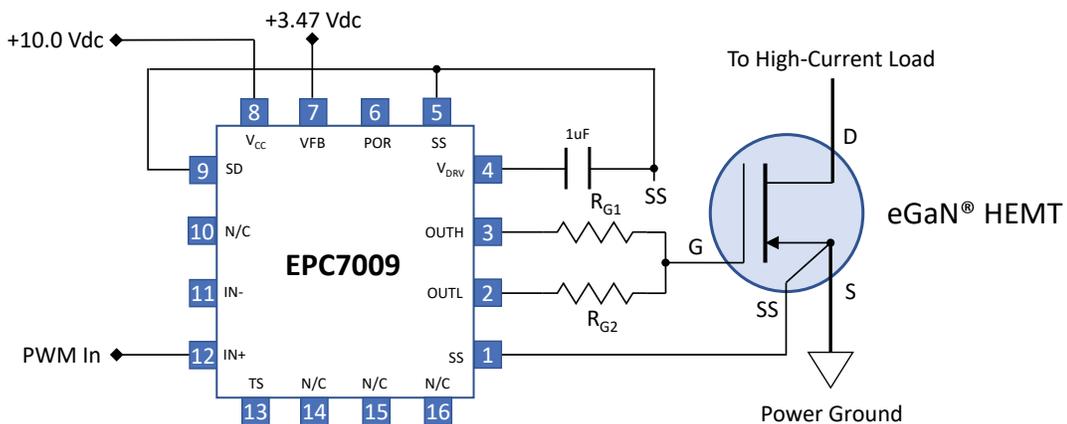
EPC7009L16SH Piinout

16 Pin QLCC SMT Package

Top (X-Ray) View   **Bottom (Pad) View**
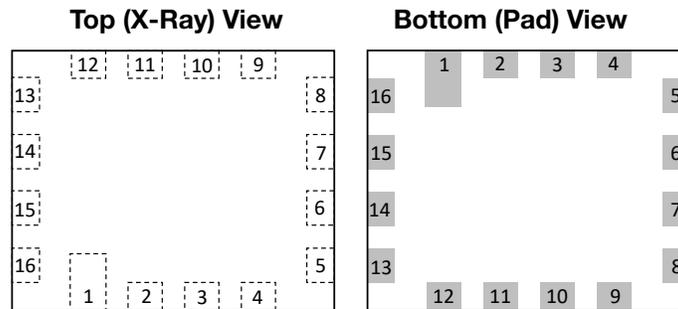
EPC7009L16SH Pin Descriptions and Functionality

Pin #	Pin Name	(I)nput, (O)utput, (P)ower	Pin Function
1	SS	P	Gate driver ground return that is connected to the "Source Sense" (SS) pad on EPC Space eGaN HEMTs. Keep the connection from the SS pin to the Source pad as short as possible. The substrate of the IC is also connected to the SS pin.
2	OUTL	O	Gate driver high peak current pull-down output. When ON, the OUTL output is pulled down to the SS potential. In most applications this pin should be connected directly to the gate pad of EPC Space eGaN HEMTs. Keep the connection from the OUTL pin to the Gate pad as short as possible.
3	OUTH	O	Gate driver high peak current pull-up output. When ON, this output is pulled up to the VDRV potential. A low value resistor (10 W, maximum) may be connected in series with the OUTH pin and the Gate pad of EPC Space eGaN HEMTs in order to slow down the rise time of the HEMT being driven. Keep the connection from the OUTH pin (and through the optional gate resistor) to the Gate pad as short as possible.
4	VDRV	P	Regulated 5.0 V supply voltage. Connect a 1.0 µF, minimum, bypass capacitor from V to SS.
5	SS	P	Gate driver ground return that is connected to the "Source" pad on EPC Space eGaN HEMTs. Keep the connection from the SS pin to the Source pad as short as possible. The substrate of the IC is also connected to the SS pin.
6	POR	I/O	Power-On-Reset output. IC is active when POR is logic 0. Connect to SS to disable the POR function. (When POR is logic 1, it will disable the gate driver.)
7	VFB	I	Adjustable reference input voltage for linear regulator.
8	VCC	P	External 10 V power supply connection referenced to SS.
9	SD	I	Internal linear regulator shutdown input (low ON, high OFF).
10	NC	--	No connection
11	IN-	I	Negative logic input, level referenced to SS. Output will be high when IN- < V_{IL} with IN+ = V_{DRV}. This input has an internal pull-down resistor to SS.
12	IN+	I	Positive logic input, level referenced to SS. Output will be high when IN+ > V_{IH} with IN- = SS or floating. This input has an internal pull-down resistor to SS.
13	NC	--	No connection
14	NC	--	No connection
15	NC	--	No connection
16	NC	--	No connection

Figure 1. EPC7009 Simplified Functional Block Diagram

Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions	Value	Units
V_CC - SS	Input Supply Voltage	16	V
V_DRV - SS	Regulated Gate Driver Voltage	6	
IN+ - SS, IN- - SS, SD – SS POR - SS	Logic Input Voltage Range	-1.5 to 6	
VFB - SS	Regulator Feedback Adjustment Voltage Range	-1.5 to 6	
TS - SS	Temperature Sensor Resistor Input Voltage Range	-1.5 to 6	
T_STG	Storage Junction Temperature Range	-55 to +150	°C
T_J	Operating Junction Temperature Range	-55 to +125	
T_C	Case Operating Temperature Range	-55 to +110	
T_sol	Package Mounting Surface Temperature	230	
ESD	ESD Class Level (HBM)	1A	

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
R_θJA	Thermal Resistance Case-to-Ambient (Note 3)	TBD	°C/W
R_θJC	Thermal Resistance Junction-to-Case (Note 3)	TBD	

OUTL and OUTH Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter	Test Conditions		MIN	TYP	MAX	Units
V_{OL}	OUTL Low-Level Voltage	V_{DRV} = 5 V_{DC}, IN+ = 0.8 V_{DC}, I_{OUTL} = 50 µA (Note 1)	T_C = 25°C		0.05	0.1	V
			T_C = -55°C		0.05		
			T_C = 110°C		0.1	0.15	
V_{OH}	OUTH High-Level Voltage	V_{DRV} = 5 V_{DC}, IN+ = 3 V_{DC}, I_{OUTH} = -50 µA (Note 1)	T_C = 25°C	4.90	4.95		V
			T_C = -55°C	4.85	4.90	5.00	
			T_C = 110°C		4.90		
$R_{DS(on)}$	OUTL Pull-Down ON-State Resistance (V_{DRV}-OUT)	V_{DRV} = 5 V_{DC}, IN+ = 0.8 V_{DC}, I_{OUT} = 0.25 A (Notes 1, 2, 3)	T_C = 25°C		0.5		Ω
			T_C = -55°C				
			T_C = 110°C				
$R_{DS(on)}$	OUTH Pull-Up ON-State Resistance (V_{OUT}-SS)	V_{DRV} = 5 V_{DC}, IN+ = 3 V_{DC}, I_{OUT} = -0.25 A (Note 1)	T_C = 25°C		0.5		Ω
			T_C = -55°C				
			T_C = 110°C				

IN+/IN- Logic Input Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{IL}	Low Logic Level Input Voltage	V_{DRV} = 5 V_{DC}, IN+/IN- Falling (Note 4)	1.5	2.0	2.3	V
V_{IH}	High Logic Level Input Voltage	V_{DRV} = 5 V_{DC}, IN+/IN- Rising (Note 5)	2.0	2.2	2.8	
V_{HYST}	Input Logic Threshold Hysteresis	V_{IH} Rising – V_{IL} Falling	0.1	0.18	0.35	
R_{IL}	Logic Input Pull-Down Resistance	(Note 6)		5		kΩ

V_{CC}, V_{FB} and V_{DRV} Static Electrical Characteristics *(-55°C ≤ T_C ≤ 110°C unless otherwise noted)*

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{CC}	V_{CC} Operating Voltage Range		9	10	11	V
$I_{CC0\ (sleep)}$	V_{CC} Sleep Mode Quiescent Current	IN+ = 0 V_{DC}, IN- = 0 V_{DC}, EN = 5 V_{DC}	1.5	2.5	3.5	mA
$I_{CCQ\ (run)}$	V_{CC} Run Mode Quiescent Current	IN+ = 0 V_{DC}, IN- = 5 V, EN = 0 V	5.5	8	11	
$I_{CC(250k)}$	V_{CC} Total Operating Current: 250 kHz	V_{DRV} = 5 V_{DC}, IN+ = 0-5V, f_s = 250 kHz, 50% On-Time	8	10	13	
$I_{CC(1M)}$	V_{CC} Total Operating Current: 1 MHz	V_{DRV} = 5 V_{DC}, IN+ = 0-5V, f_s = 250 kHz, 50% On-Time	16	20	23	
V_{DRV}	Regulated Gate Driver Voltage	V_{DRV} to SS (Note 7)	4.50	5.00	5.75	V
V_{FB}	Linear Regulator Reference Input Voltage	V_{FB} to SS (Note 7)	3.33	3.63	3.93	
I_{DRVQ}	V_{DRV} Off State Quiescent Current	IN+ = 0 V_{DC}, IN- = 0 V_{DC}, EN = 0 VDC		7		mA
I_{DRV_250kHz}	V_{DRV} Operating Current: 250 kHz	V_{DRV} = 5 V_{DC}, IN+ = 0-5V, f_s = 250 kHz, 50% On-Time		9		
I_{DRV_1MHz}	V_{DRV} Operating Current: 1 MHz	V_{DRV} = 5 V_{DC}, IN+ = 0-5V, f_s = 250 kHz, 50% On-Time		19		

Under-Voltage Lockout Static Electrical Characteristics *(-55°C ≤ T_C ≤ 125°C unless otherwise noted)*

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
UVLO+	V_{DRV} UVLO Rising Threshold	(Note 7)	2.6	3.6	4.7	V
UVLO+ UVLO−	V_{DRV} UVLO Hysteresis to Falling Threshold		0.3	0.4	0.68	
$POR_{(th)}$	POR Threshold Voltage	I(PG) = 15 mA			0.15	

Power Driver Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter	Test Conditions		MIN	TYP	MAX	Units
$t_{d(on)}$	IN+/IN- -to-OUT Turn-ON Delay Time	VDRV = 5 VDC; COUT = 2200 pF (See Figures 2, 3, 4 and 5)			10		ns
$t_{d(off)}$	IN+/IN- -to-OUT Turn-OFF Delay Time				7		
t_r	OUT Rise Time	V_{DRV} = 5 VDC (See Figures 2, 3, 4 and 5)	C_{OUT} = 1000 pF				
			C_{OUT} = 2200 pF		3.5		
			C_{OUT} = 5100 pF				
t_f	OUT Fall Time		C_{OUT} = 1000 pF				
			C_{OUT} = 2200 pF		3.5		
			C_{OUT} = 5100 pF				

Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
PW	Minimum Pulse Width, ON or OFF	V_{DRV} = 5 V_{DC}	50			ns

Switching Figures
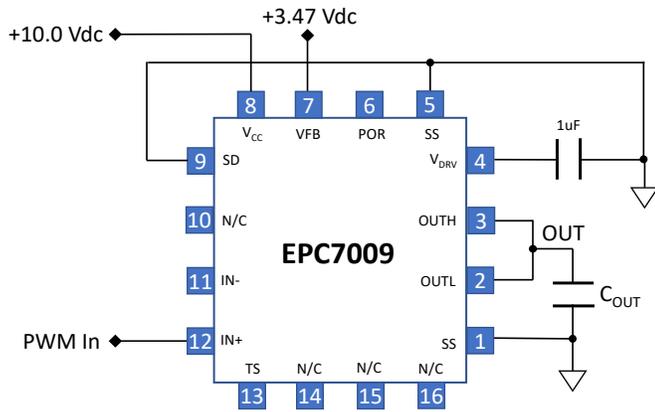
+10.0 Vdc

+3.47 Vdc

PWM In

Only pins connected during testing identified.
Pulse Generator set to 500 kHz frequency, 5% duty cycle.

Figure 2. IN+ -to-OUT Switching Time Test Circuit
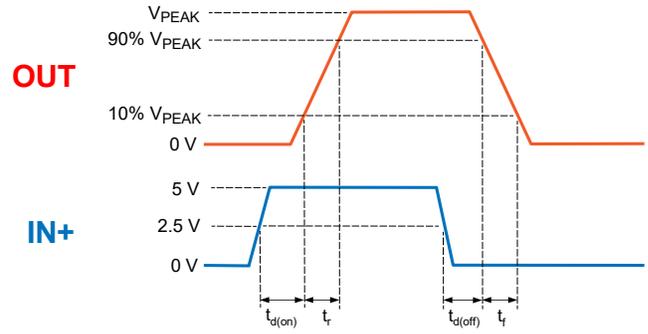
NOTE: Waveforms exaggerated for clarity and observability.

Figure 3. IN+ -to-OUT Switching Time Definition
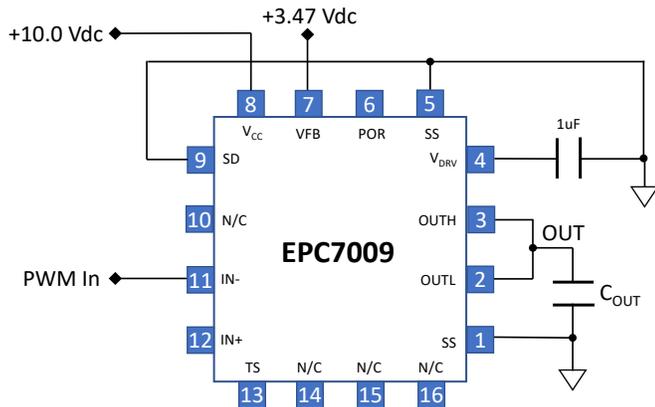
+10.0 Vdc

+3.47 Vdc

PWM In

Only pins connected during testing identified.
Pulse Generator set to 500 kHz frequency, 5% duty cycle.

Figure 4. IN- -to-OUT Switching Time Test Circuit
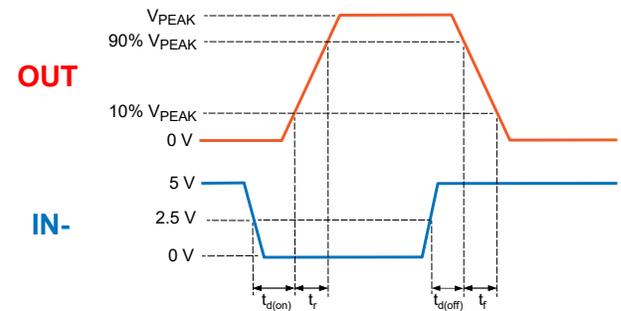
NOTE: Waveforms exaggerated for clarity and observability.

Figure 5. IN- -to-OUT Switching Time Definition

Radiation Characteristics

The EPC7009 is a Radiation Hardness-Assured Single Output GaN Driver Integrated Circuit.

- EPC Space's EPC7009 internally utilizes eGaN HEMT technology designed, fabricated and tested per Mil-Std-883 Method 1019 for total ionizing dose validation.

- The EPC7009 has been found to be immune to Single Event Effect and Upset when irradiated with gold ion Au at a surface LET (Si) of 84 MeV/mg/cm^2 at TAMU.

Specification Notes

1.) V_{DRV} = +5 V_{DC}, SS = 0 V_{DC}.

2.) Measured using 4-Wire (Kelvin) sensing techniques.

3.) Guaranteed by design. Not tested in production.

4.) When the logic input (IN+) is at the low input voltage level the OUTL output is guaranteed to be ON (~SS potential) and the OUTH output is guaranteed to be OFF (open).

5.) When the logic input (IN+) is at the high input voltage level the OUTH output is guaranteed to be ON (~V_{DRV} potential) and the OUTL output is guaranteed to be OFF (open).

6.) Pull-down to SS for IN+ and pull-up to V_{DRV} for IN-.

7.) The regulated output voltage, V_{DRV}, is 1.44 x V_{FB}, nominal. For a nominal 5 V_{DC} output for V_{DRV}, V_{FB} = 3.47 V_{DC}. The gate driver potential V_{DRV} may be adjusted to any value within the V_{FB} specified range.

EPC7009 Operational Truth Table

The truth table for the logic inputs and the power supply UVLO circuit is shown in the following table. In the following table, OUT is the combined driver output when OUTL and OUTH are connected together.

All conditions in the table are valid when V_{BIAS} and V_{DRV} are greater than UVLO+. When V_{CC} and V_{DRV} are less than ULVO+ rising or UVLO+ falling, OUT is in the low (L) state, approximately the SS potential, regardless of the state of either logic input.

| IN+	IN-	OUT
0	0	L
1	0	H
0	1	L
1	1	L

Application Information

The following figures detail the suggested applications for the EPC7009 integrated circuit. For all applications, please refer to the following sections for proper power supply bypassing and layout recommendations and criteria.

In all the following figures, only the pins that are considered or that require connection are identified.
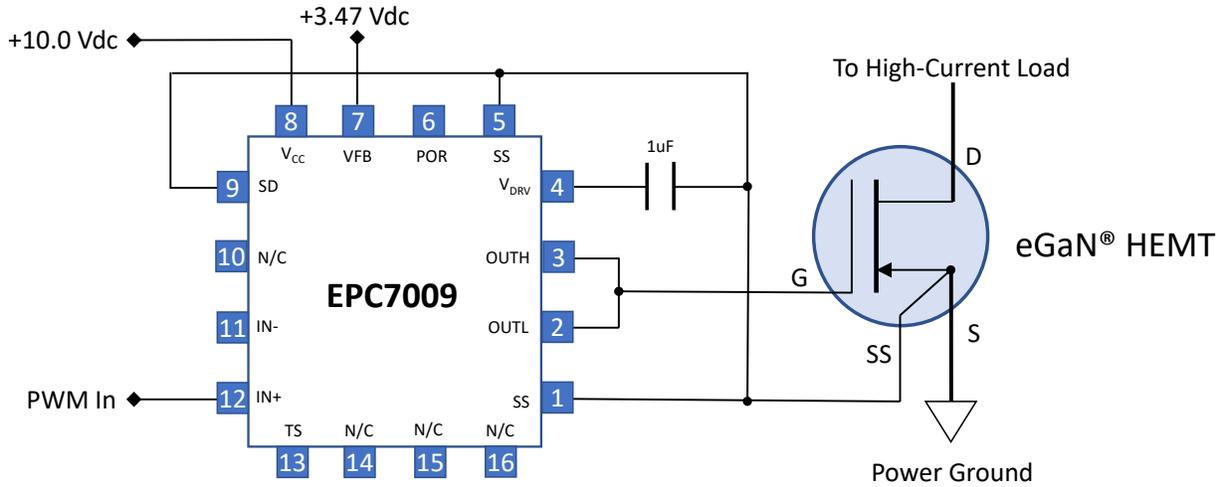

Note: Keep Out-to-Gate and SS-to-Source-Sense connections as short as possible.

Figure 7. Non-Inverting Mode Low-Side Driver and EPC Space eGaN® HEMT
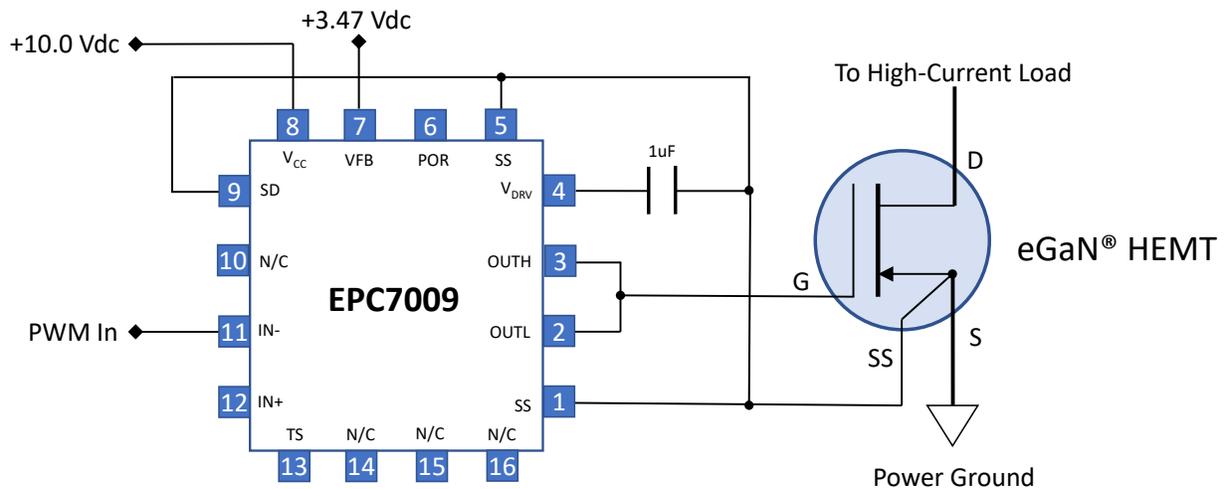
Note: Keep Out-to-Gate and SS-to-Source-Sense connections as short as possible.

*Figure 8. Inverting Mode Low-Side Driver and EPC Space eGaN® HEMT*
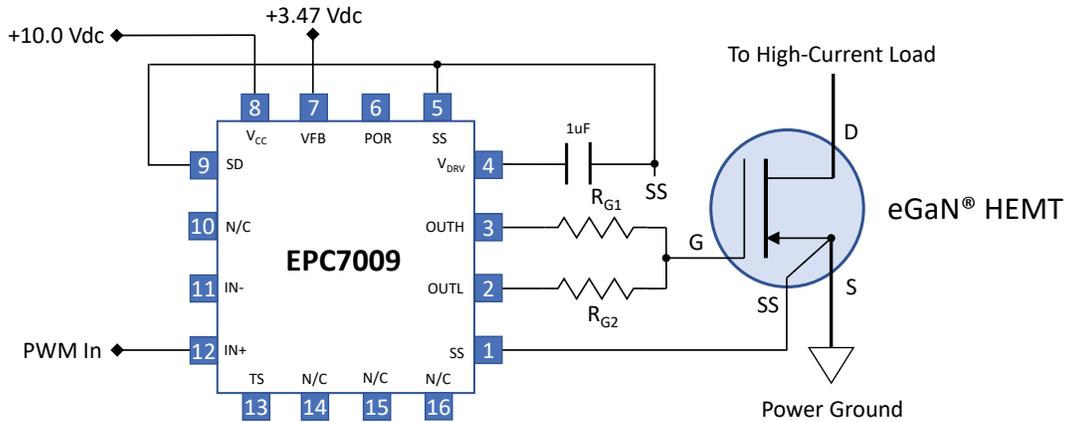
Note: Make all OUTH-to-RG1, OUTL-to-RG2, the tie point of RG1/RG2-to-Gate and
SS-to-Source Sense connections of equal length and as short as possible.
RG1/RG2 are 20 Ω, maximum

*Figure 9. Non-Inverting Mode Low-Side Driver and EPC Space
eGaN® HEMT with Gate Damping/Slow-Down Resistors*

In Figure 9 resistor RG1 is used to control the rise time of the eGaN® HEMT and resistor RG2 is used to control the fall time. Such resistors are often utilized to reduce EMI or to minimize voltage overshoot and ringing on the V_{DD} bus local to the high current being switched by the eGaN HEMT.
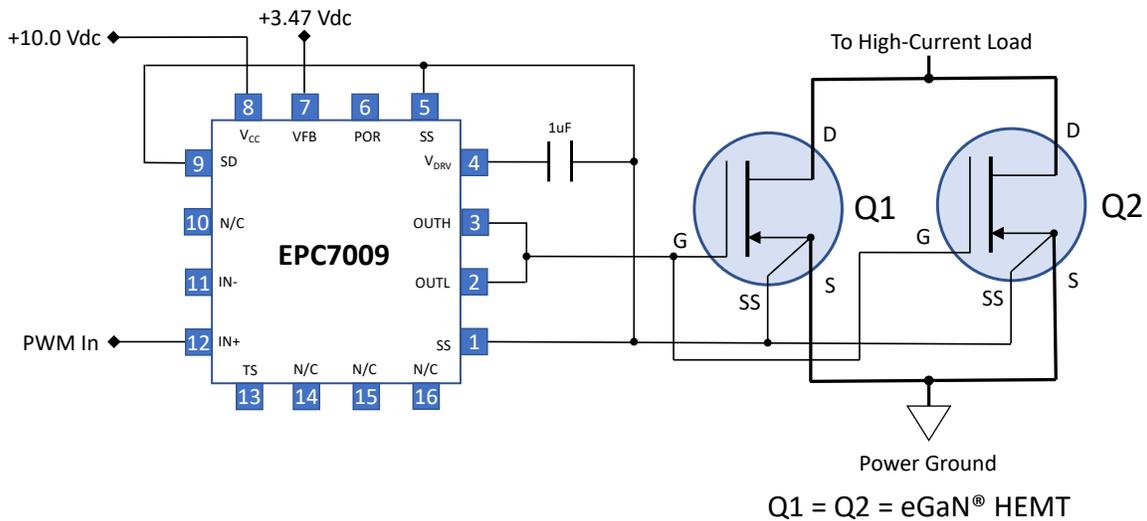
Note: Make all OUTH/OUTL-to-Gate, SS-to-Source Sense and Source connections
as short as possible. Also keep the Drain connections as short as physically possible.

Figure 10. Non-Inverting Mode Low-Side Driver Driving Multiple, Parallel EPC Space eGaN® HEMTs

For parallel the parallel HEMT configuration as shown in Figure 10, the number of HEMT devices that may be driven in parallel is determined by the C_{ISS} of the individual HEMTs and the capacitive drive capability of the EPC7009 gate driver integrated circuit.
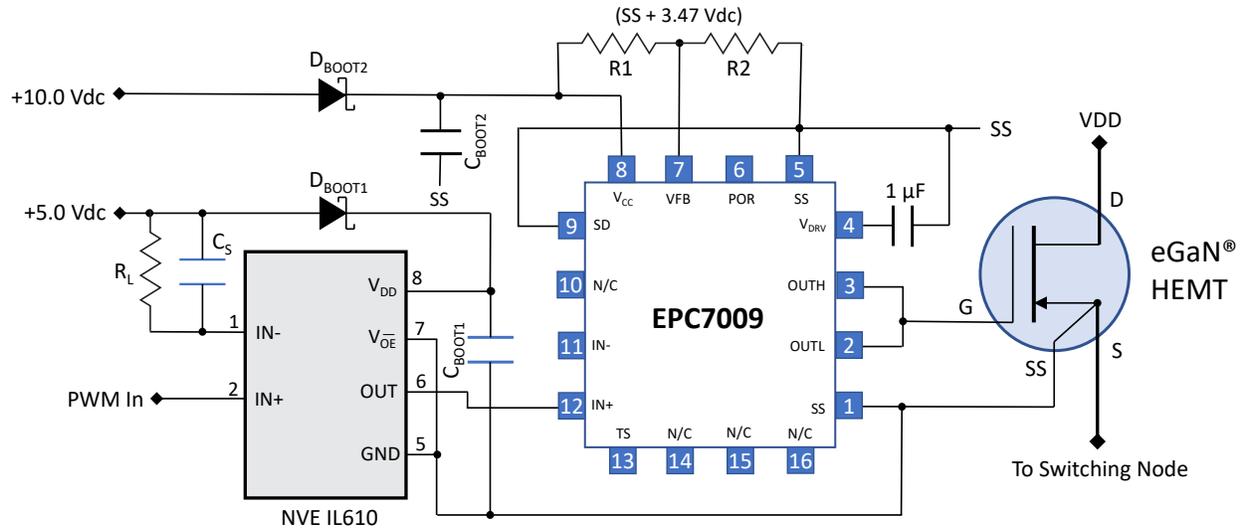
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Note: Make all OUTH/OUTL-to-Gate, SS-to-Source Sense and Source connections as short as possible.
Also keep the Drain connections as short as physically possible. The SS node may be treated
as a local etch plane in the area of the IL610, the EPC7009 and the eGaN® HEMT.
Circuit shown utilizes dual bootstrapping: one for the NVE IL610 and one for the EPC7009.

Figure 11. Non-Inverting Mode Low-Side Driver Driving Multiple, Parallel EPC Space eGaN® HEMTs

Package Outline Dimensions
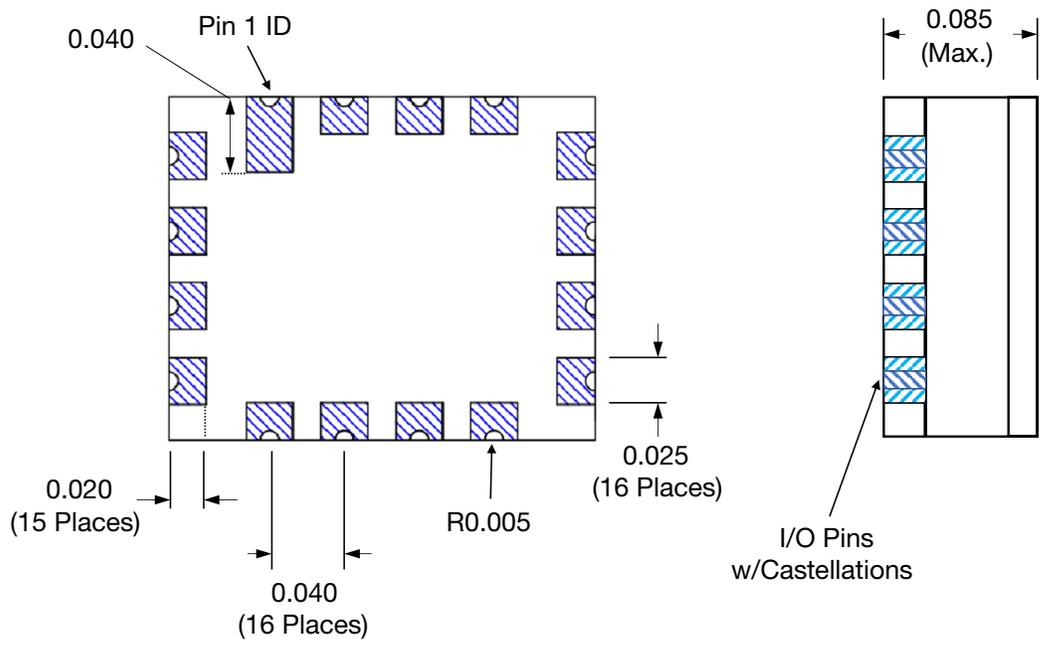
Figure 12. EPC7009L16SH Package Outline Dimensions

Recommended PCB Solder Pad Configuration

To prevent damage to the internal circuitry it is important that the EPC7009L16SH integrated circuit be soldered to the PCB motherboard using SN63 (or equivalent) solder. The recommended PCB pad dimensions and locations are shown in Figure 13.

All dimensions are shown in inches.
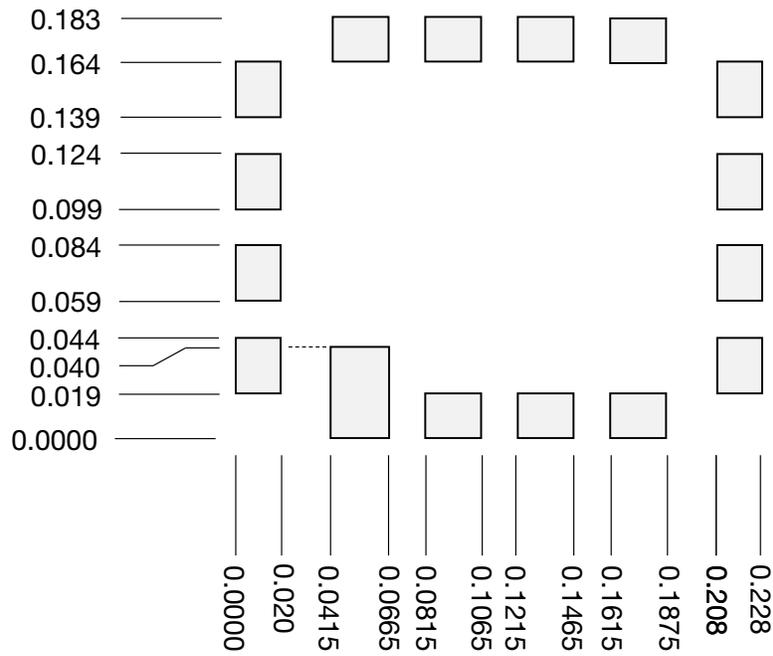
Figure 13. Recommended PCB Solder Pad Configuration (Top View)

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Revisions

Datasheet Revision	Product Status
REV P#	Proposal/development
REV Q#	Characterization and Qualification
	Production Released

Information subject to change without notice.
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