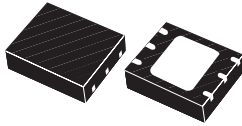
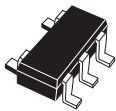


## 200 mA low dropout LDO

DFN 2x2 6L  
Wettable Flanks

SOT23 5L

Maturity status link

LDH40

## Features

- AEC-Q100 grade 1 qualified
- Operating temperature range:  $-40\text{ }^{\circ}\text{C} < T_J < +150\text{ }^{\circ}\text{C}$
- Input voltage from 3.3 V to 40 V
- Dropout voltage (700 mV typ. at 200 mA load)
- Low ground current (2  $\mu\text{A}$  typ. at no load)
- ADJ from 1.2 V to 22 V
- Output voltage tolerance: 0.5% at 25  $^{\circ}\text{C}$
- 200 mA guaranteed output current
- Power Good
- Logic-controlled electronic shutdown
- Internal current limit
- Thermal shutdown
- Output active discharge function
- Package options:
  - DFN 2x2 6L WF for automotive grade
  - SOT23 5L and DFN 6L for industrial

## Applications

- EV powertrain
- Body control modules
- Always-on battery connected application
- Infotainment and instrument cluster
- ADAS

## Description

LDH40 is a high accuracy voltage regulator designed to be directly connected to a car battery in automotive applications, or a generic battery connected in industrial applications. Extended input voltage up to 40 V makes the device capable to support a load dump transient, typical in automotive systems. Ultra-low quiescent current at light load increases the battery operation lifetime in always-on-standby systems.

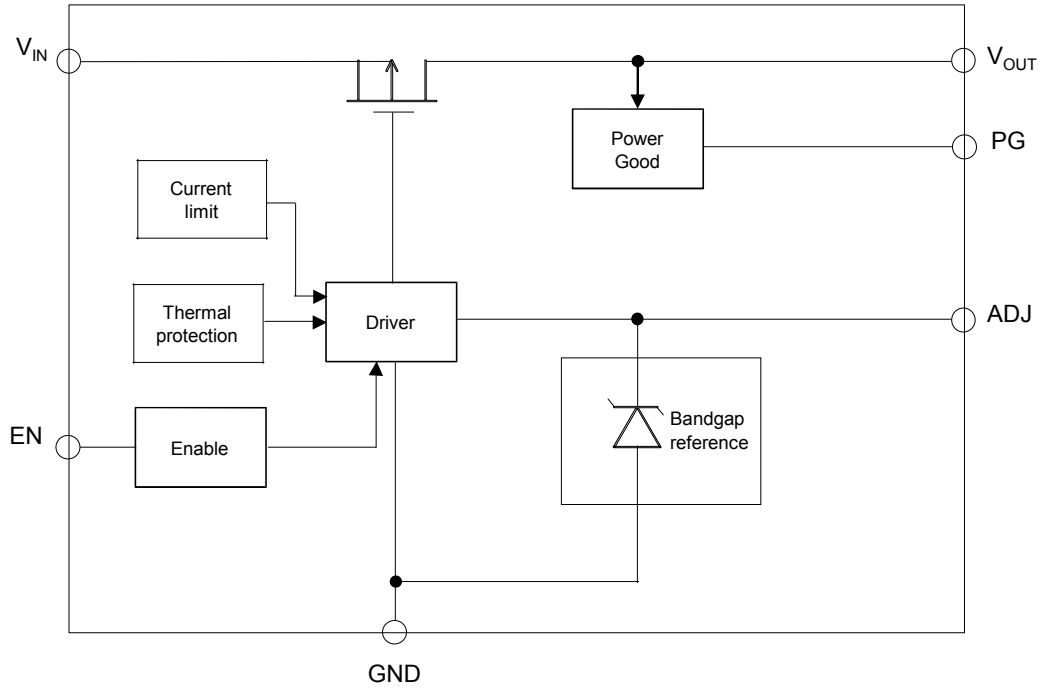
The device is stabilized with a small ceramic capacitor on the input and output.

An enable logic control function puts the LDH40 in shutdown mode allowing a total current consumption lower than 0.3  $\mu\text{A}$ . Thermal protection is also included.

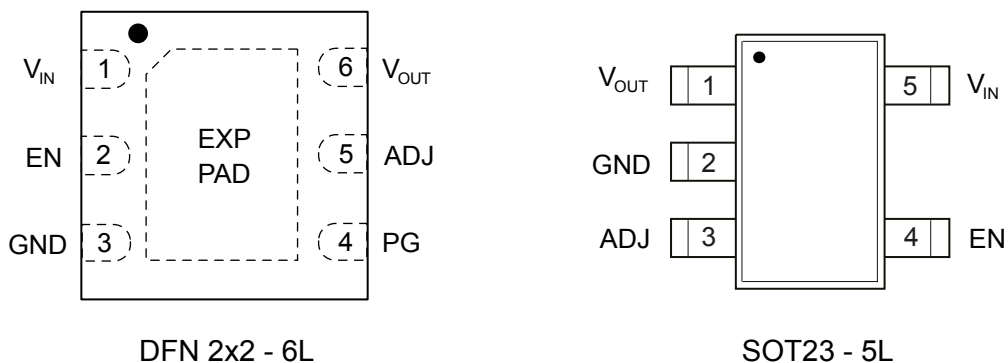
The device is available in automotive grade in a very small footprint DFN package with wettable flank, allowing the maximum space saving in the PCB (printed circuit board) design and AOI (automated optical inspection).

# 1 Diagram

Figure 1. Block diagram adjustable version



## 2 Pin configuration

**Figure 2. Pin connection (top view)**

**Table 1. Pin description DFN 2x2 6L**

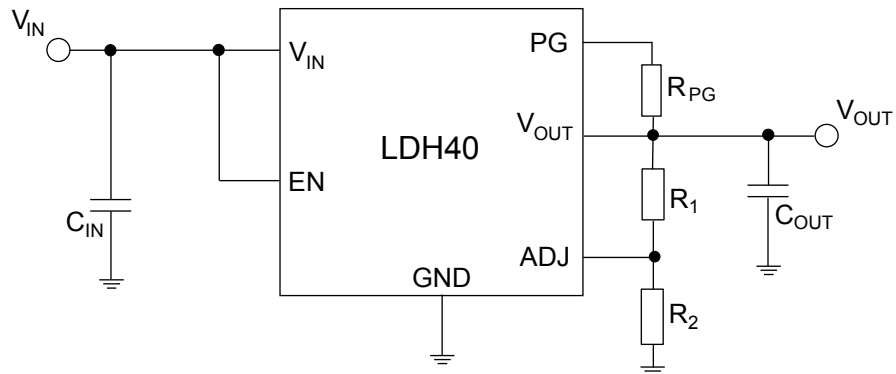
DFN 2x2-6L	Symbol	Function
1	$V_{IN}$	Input voltage
2	EN	Enable pin logic input: set $V_{EN}$ = high to turn ON the device $V_{EN}$ = low to turn off the device Do not leave this pin floating
3	GND	Ground
4	PG	Power Good
5	ADJ	ADJ: adjust pin on the adjustable version Connect to resistor divider to set the output voltage
6	$V_{OUT}$	Output voltage
Exp PAD	Exposed pad	Connect to GND

**Table 2. Pin description SOT 23 5L**

SOT23 5L	Symbol	Function
1	$V_{OUT}$	Output voltage
2	GND	Ground
3	ADJ	Adjust pin
4	EN	Enable pin logic input: set $V_{EN}$ = high to turn ON the device $V_{EN}$ = low to turn OFF the device Do not leave this pin floating
5	$V_{IN}$	Input voltage

### 3 Typical application circuit

**Figure 3. Typical application for the adjustable version**



*Note:* PG pin only for DFN version.

**Table 3. Typical application components**

Symbol	Value	Description	Note
$C_{IN}$	1 $\mu$ F	Input capacitor	Ceramic type
$C_{OUT}$	From 1 to 200 $\mu$ F	Output capacitor	Ceramic type
ESR	From 5 m $\Omega$ to 10 $\Omega$		
$R_1$	2 M $\Omega$ max	Output voltage side resistor	
$R_2$	2 M $\Omega$ max	Ground side resistor	
$R_{PG}$	From 10 K $\Omega$ to 2 M $\Omega$		

Including component derating.

## 4 Absolute maximum ratings

Stressing the device above the ratings listed in Table 4. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of these specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{IN}$	Input voltage	-0.3 to +42	V
$V_{OUT}$	Output voltage	-0.3 to +25	V
$V_{ADJ}$	Adjust voltage	-0.3 to +3	V
$V_{EN}$	Enable input voltage	-0.3 to $V_{IN}$	V
$V_{PG}$	Power Good	-0.3 to +25	V
$I_{OUT}$	Output current	Internally limited	A
$T_{STG}$	Storage temperature range	-40 to +150	°C
$T_{JOP}$	Operating junction temperature range	-40 to +150	°C

**Table 5. Thermal data**

Symbol	Parameter	DFN 2x2 6L	SOT23 5L	Unit
$R_{thJA}$	Thermal resistance junction-ambient <sup>(1)</sup>	62	200	°C/W

1.  $R_{thJA}$  for DFN6 is based on a 4-layer JEDEC PCB (2S2P) test board with two thermal vias.

**Table 6. ESD performance**

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM on corner pins of DFN WF	750	V
		CDM inner pins of DFN WF	500	V
		CDM industrial packages	500	V

## 5 Electrical characteristics

$V_{IN} = V_{OUT (NOM)} + 1 \text{ V}$  or  $3.3 \text{ V}$  (whichever is greater);  $I_{OUT} = 1 \text{ mA}$ ;  $C_{IN} = 4.7 \mu\text{F}$ ,  $C_{OUT} = 10 \mu\text{F}$ ;  $V_{EN} = V_{IN}$ ; typical values are at  $T_J = 25 \text{ }^\circ\text{C}$ ; min/max values are at  $-40 \text{ }^\circ\text{C} \leq T_J \leq 150 \text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 7. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating input voltage		$V_{OUT} + V_{DROP}$		40	V
$V_{IN (UVLO)}$	Undervoltage lockout	Rising edge		2.6	3.0	V
		Hysteresis		0.35		
$V_{REF}$	Reference voltage for adjustable devices	$T_J = 25 \text{ }^\circ\text{C}$		1.2		V
$V_{OUT}$	Output voltage accuracy	All versions, $T_J = 25 \text{ }^\circ\text{C}$	-0.5		+0.5	%
		$V_{OUT (NOM)} + 1 \text{ V} \leq V_{IN} \leq 32 \text{ V}$ ; $I_{OUT} = 1 \text{ mA}$ to $200 \text{ mA}$ ; $-40 \text{ }^\circ\text{C} \leq T_J \leq 150 \text{ }^\circ\text{C}$	-2.5		+2.5	%
$\Delta V_{OUT-IN}$	$V_{IN}$ static regulation	$V_{OUT (NOM)} + 1 \text{ V} \leq V_{IN} \leq 32 \text{ V}$		0.01	0.03	% / V
$\Delta V_{OUT-LOAD}$	Static load regulation	$I_{OUT} = 1 \text{ mA}$ to $200 \text{ mA}$		3.0		mV
$V_{DROP}$	Dropout voltage	$I_{OUT} = 200 \text{ mA}$ ; $V_{OUT} = 97\%$ of $V_{OUT (NOM)}$		700	1000	mV
$I_{LIM}$	Output current limit	$V_{OUT} = 90\%$ $V_{OUT (NOM)}$	350	650	1000	mA
$I_{ADJ}$	ADJ pin operating current			0.1	0.5	$\mu\text{A}$
$I_Q$	Quiescent current during regulation	$V_{IN}$ from $3.3 \text{ V}$ to $40 \text{ V}$ no load		2	5	$\mu\text{A}$
		10 mA		50		
		100 mA		150		
		200 mA		200	500	
$I_{Q\_OFF}$	Standby current	$V_{IN} = 32 \text{ V}$		0.3	1.2	$\mu\text{A}$
$V_{EN}$	Enable input logic low	$V_{IN}$ up to $40 \text{ V}$			0.7	V
	Enable input logic high	$V_{IN}$ up to $40 \text{ V}$	2.0			
$I_{EN}$	Enable pin input current	$V_{EN}$ from $2 \text{ V}$ to $40 \text{ V}$		0.01	0.1	$\mu\text{A}$
$V_{PG\_OK}$	Power Good output threshold, rising		93		98	%Vout <sup>(1)</sup>
$V_{PG\_NOK}$	Power Good output threshold, falling		86		95	
	Power Good hysteresis		30	70		mV
$V_{PG\_L}$	Power Good output voltage low	$I_{SINK\_MAX} = 6 \text{ mA}$ , open drain output			0.4	V
$T_{ON}$	Turn on time	From assertion of $V_{EN}$ to $0.98\% * V_{OUT}$ . $V_{OUT (NOM)} - V_{OUT (NOM)} = 1.0 \text{ V}$		1		ms
SVR	Supply voltage rejection	$V_{IN} = 5 \text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2 \text{ V}$ ; freq = $1 \text{ kHz}$ $I_{OUT} = 10 \text{ mA}$ ; $V_{OUT (NOM)} = 1.2 \text{ V}$		65		dB
		$V_{IN} = 15 \text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.2 \text{ V}$ ; freq = $1 \text{ kHz}$ ; $I_{OUT} = 10 \text{ mA}$ ; $V_{OUT (NOM)} = 1.2 \text{ V}$		70		dB

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	e <sub>N-ADJ</sub> output noise voltage	V <sub>IN</sub> = 3 V; V <sub>OUT (NOM)</sub> = 1.2 V; 10 Hz to 100 kHz, I <sub>OUT</sub> = 1 mA		100		μV <sub>RMS</sub>
		V <sub>IN</sub> = 12 V; V <sub>OUT (NOM)</sub> = 3.3 V; 10 Hz to 100 kHz, I <sub>OUT</sub> = 1 mA		300		μV <sub>RMS</sub>
R <sub>ON</sub>	Output voltage discharge MOSFET			150		Ω
T <sub>SHDN</sub>	Thermal shutdown			175		°C
	Hysteresis			20		

1. The Power Good threshold is calculated as a percentage of the measured V<sub>out</sub>

## 6 Application information

### 6.1 $V_{IN}$ pin voltage requirements

The LDH40 is a low-dropout linear voltage regulator equipped with a low-RDS-(on) P-channel MOSFET used as a pass-element. The device internal circuit is able to start with an input voltage as low as 3.3 V.

### 6.2 Output discharge function

LDH40 embeds an open drain that allows the output capacitor to discharge, at about 150 Ohm, when the enable pin goes to zero.

### 6.3 Current limitation

The LDH40 is protected against short circuits on the output. The load current is limited to the maximum value of  $I_{LIM}$  when  $V_{OUT}$  is equal to 90% of its nominal value.

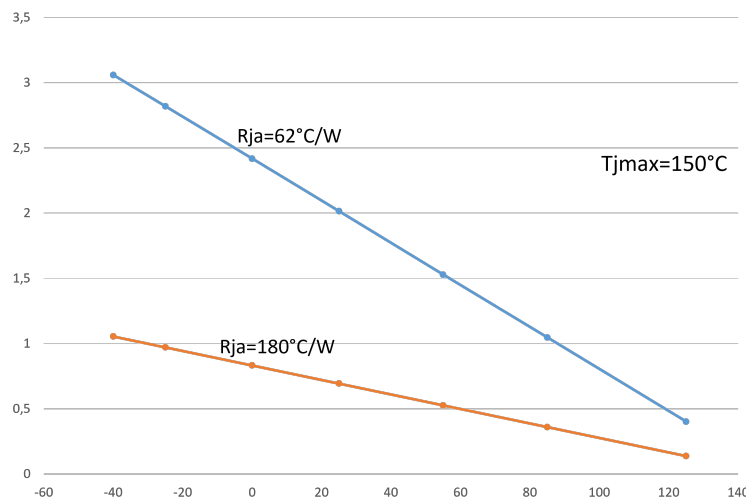
### 6.4 Thermal protection

Thermal protection acts when the junction temperature reaches 175 °C typical. At this point, the output of the IC shuts down. As soon as the junction temperature falls below the thermal hysteresis value, the device starts working again.

In order to calculate the maximum power that the device can dissipate, keeping the junction temperature below the maximum operating value, the following formula is used:

$$P_{DMAX} = (150 - T_{AMB}) / R_{thJA} \quad (1)$$

**Figure 4. Derating curve**



### 6.5 Input and output capacitors

The LDH40 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used, however the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR overtemperature.

It is recommended to put the input/output capacitors as close as possible to the relative pins. The LDH40 requires a  $V_{IN}$  capacitor with a minimum value of 1  $\mu$ F minimum.

The control loop is designed to be stable with any good quality output ceramic capacitor (such as X5R/X7R types) with a minimum value of 1.0  $\mu$ F and equivalent series resistance in the [5 m $\Omega$  to 10  $\Omega$ ] range. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region.



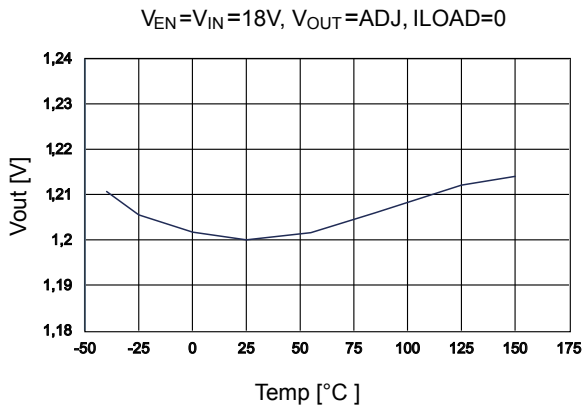
## 6.6 Power Good output

The LDH40 features a Power Good open drain output. The pin is High-Z when the output voltage is within the valid range or when the device is disabled (EN = LOW). The pin is pulled low when the output voltage is below the minimum PG threshold (see  $V_{PG\_OK}$   $V_{PG\_NOK}$  parameters).

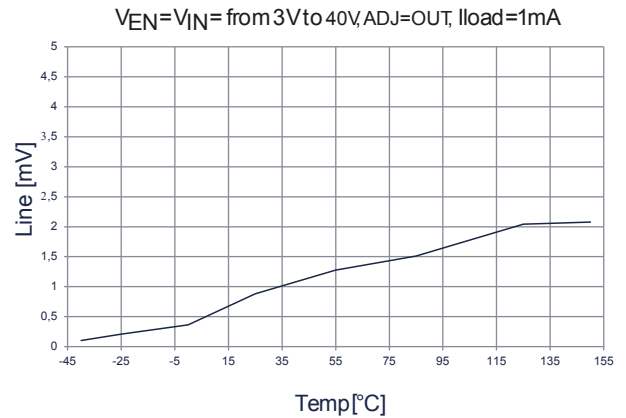
## 7 Typical characteristics

$C_{IN} = 4.7 \mu\text{F}$ ;  $C_{OUT} = 10 \mu\text{F}$

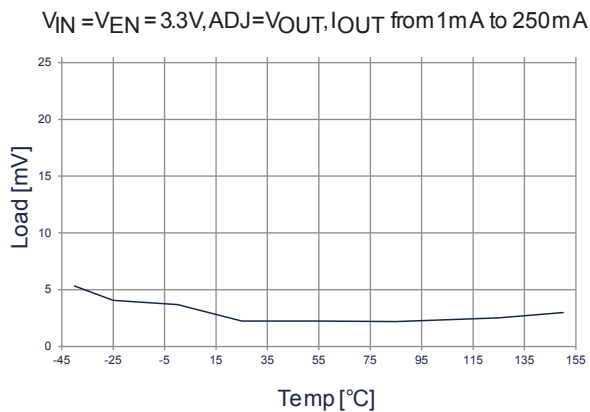
**Figure 5. Output voltage vs. temperature**



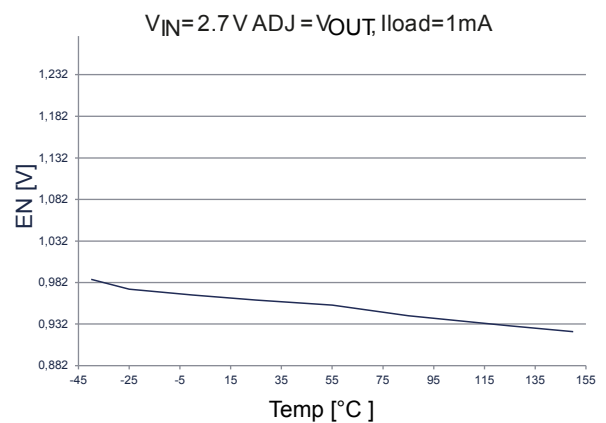
**Figure 6. Line regulation vs. temperature**



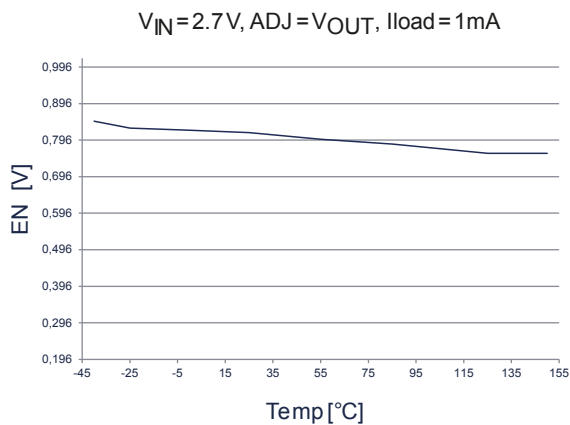
**Figure 7. Load regulation vs. temperature**



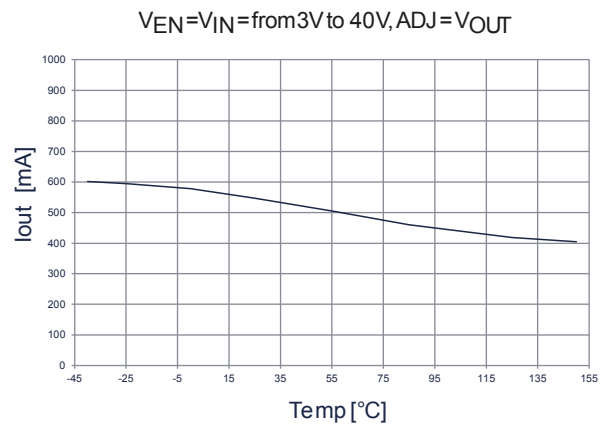
**Figure 8. Enable threshold ON**



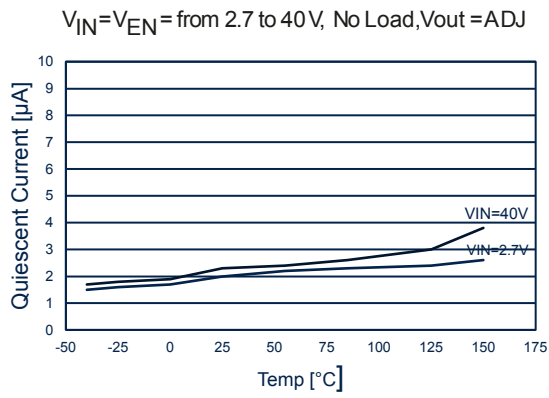
**Figure 9. Enable threshold OFF**



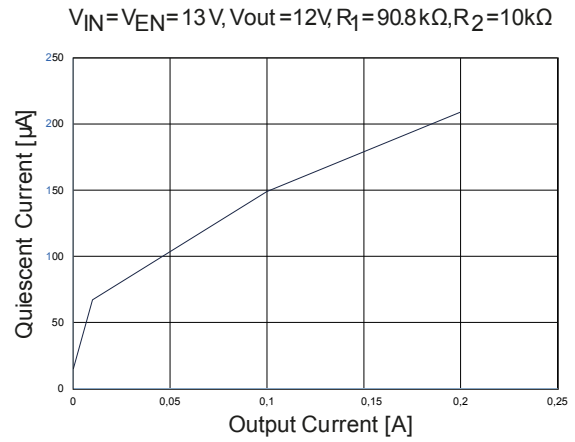
**Figure 10. Output current limit**



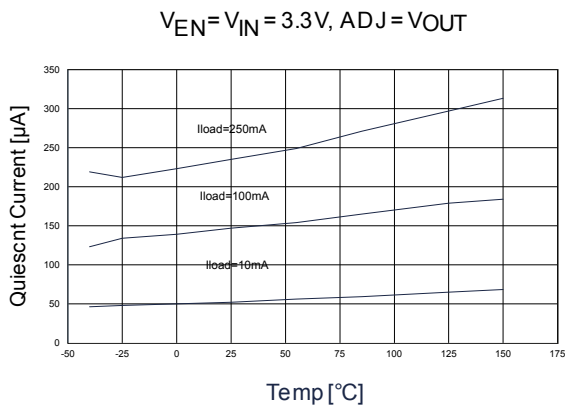
**Figure 11. Quiescent current vs. input voltage**



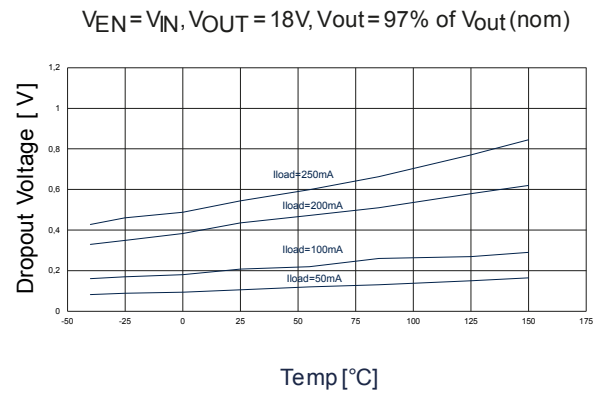
**Figure 12. Quiescent current vs. output current**



**Figure 13. Quiescent current vs. temperature**

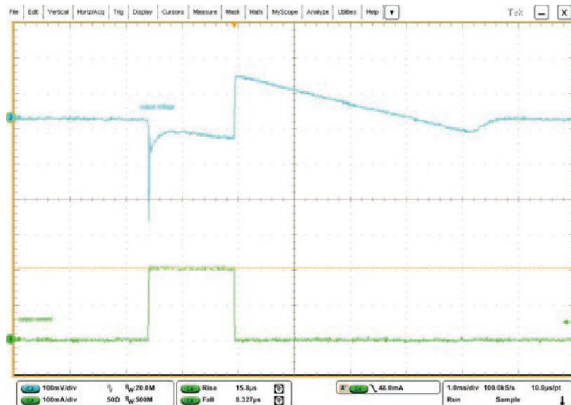


**Figure 14. Dropout voltage vs. temperature**



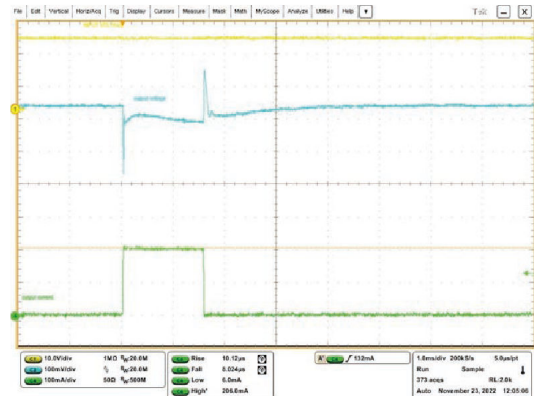
**Figure 15. Load transient  $V_{EN} = 2V$**

$V_{EN}$  = 2V,  $V_{IN}$  = 22V,  $I_{OUT}$  = from 100 $\mu$ A to 200mA and viceversa,  $V_{OUT}$  = 18V,  $t_r$  =  $t_f$  = 5 $\mu$ s



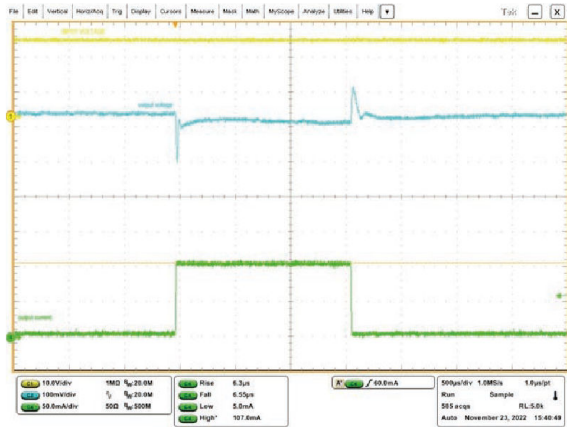
**Figure 16. Load transient  $V_{EN} = 1V$**

$V_{EN}$  = 1V,  $V_{IN}$  = 22V,  $I_{OUT}$  = from 10mA to 200mA and viceversa,  $V_{OUT}$  = 18V,  $t_r$  =  $t_f$  = 5 $\mu$ s



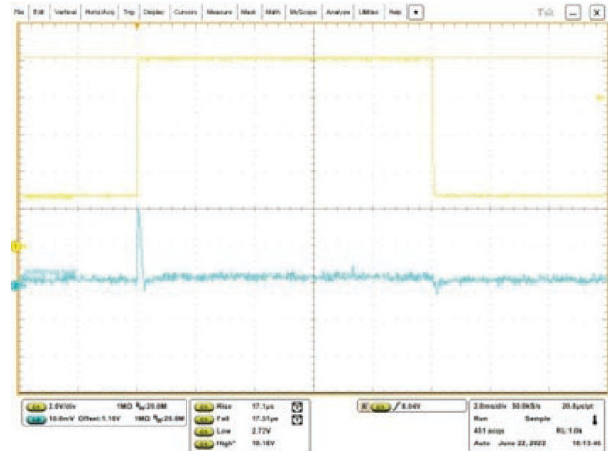
**Figure 17. Load transient**

$V_{EN}=1V$ ,  $V_{IN}=22V$ ,  $I_{OUT}$ =from 100mA to 10mA,  $V_{OUT}=18V$ ,  $t_r=t_f=5\mu s$



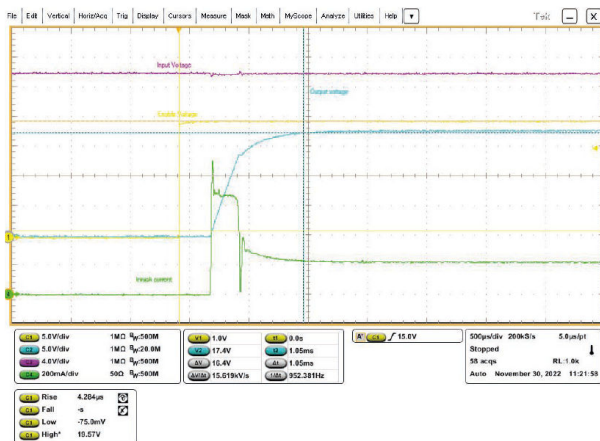
**Figure 18. Line transient**

$V_{IN}=V_{EN}=2.7V$  to 10V,  $t_r=t_f=1\mu s$ ,  $ADJ=V_{OUT}$ ,  $I_{OUT}=1mA$



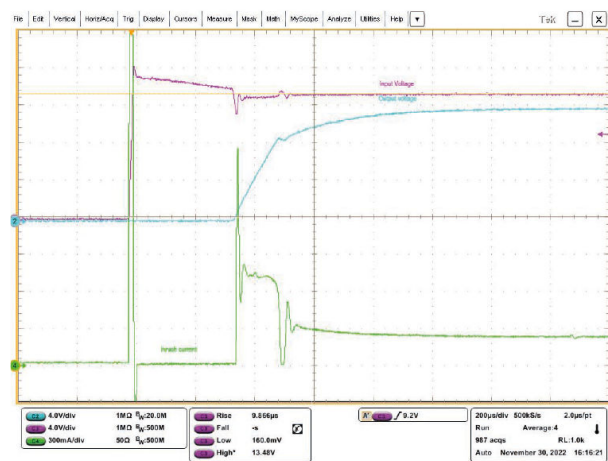
**Figure 19. Turn on time**

Turn on/off with enable  $V_{IN}=22V$ ,  $V_{OUT}=18V$ ,  $V_{EN}$ =from 0 to 20V,  $I_{OUT}=200mA$



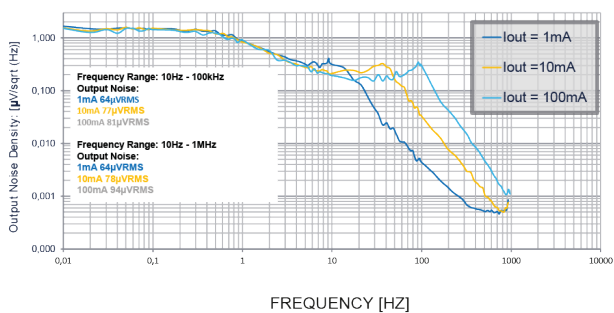
**Figure 20. Turn on time**

$V_{IN}=V_{EN}$ =from 0 to 13V,  $V_{OUT}=12V$ ,  $t_{rise}=10\mu s$ ,  $I_{OUT}=200mA$



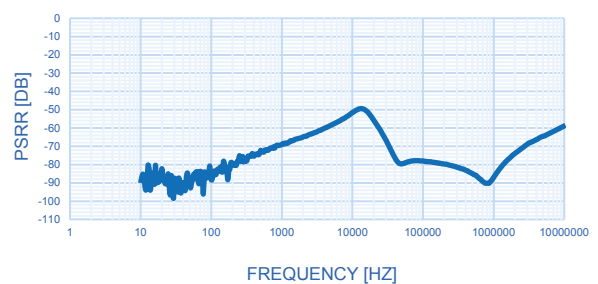
**Figure 21. Spectral noise density vs. frequency**

$V_{EN}=1V$ ,  $V_{OUT}=1.2V$ ,  $V_{IN}=3V$



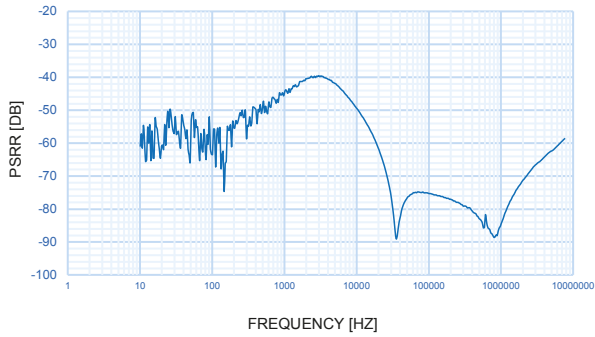
**Figure 22. PSRR vs. frequency  $V_{IN}=5V$**

$V_{EN}=2V$ ,  $V_{OUT}=1.2V$ ,  $V_{IN}=5V$ ,  $V_{ripple}=200mVpkpk$ ,  $I_{load}=1mA$



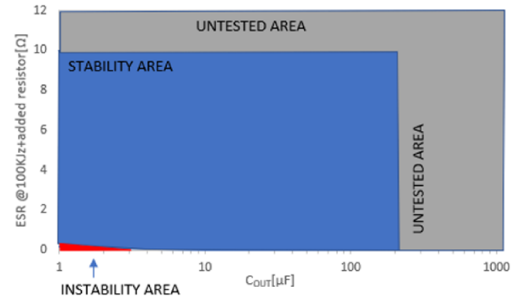
**Figure 23. PSRR vs. frequency  $V_{IN} = 19\text{ V}$**

$V_{EN} = 2\text{ V}$   $V_{OUT} = 18\text{ V}$   $V_{IN} = 19\text{ V}$   $V_{ripple} = 200\text{ mV pkpk}$   $I_{load} = 1\text{ mA}$



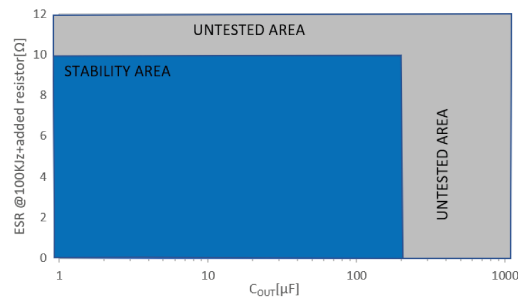
**Figure 24. Stability plane for  $V_{OUT} = 1.2\text{ V}$**

$V_{EN} = 2\text{ V}$   $V_{in} = \text{from } 3\text{ V to } 40\text{ V}$   $I_{out} = \text{from } 100\text{ }\mu\text{A to } 200\text{ mA}$



**Figure 25. Stability plane for  $V_{OUT} = 18\text{ V}$**

$V_{EN} = 2\text{ V}$   $V_{in} = \text{from } 19\text{ V to } 40\text{ V}$   $V_{OUT} = 18\text{ V}$ ,  $I_{out} = \text{from } 100\text{ }\mu\text{A to } 200\text{ mA}$

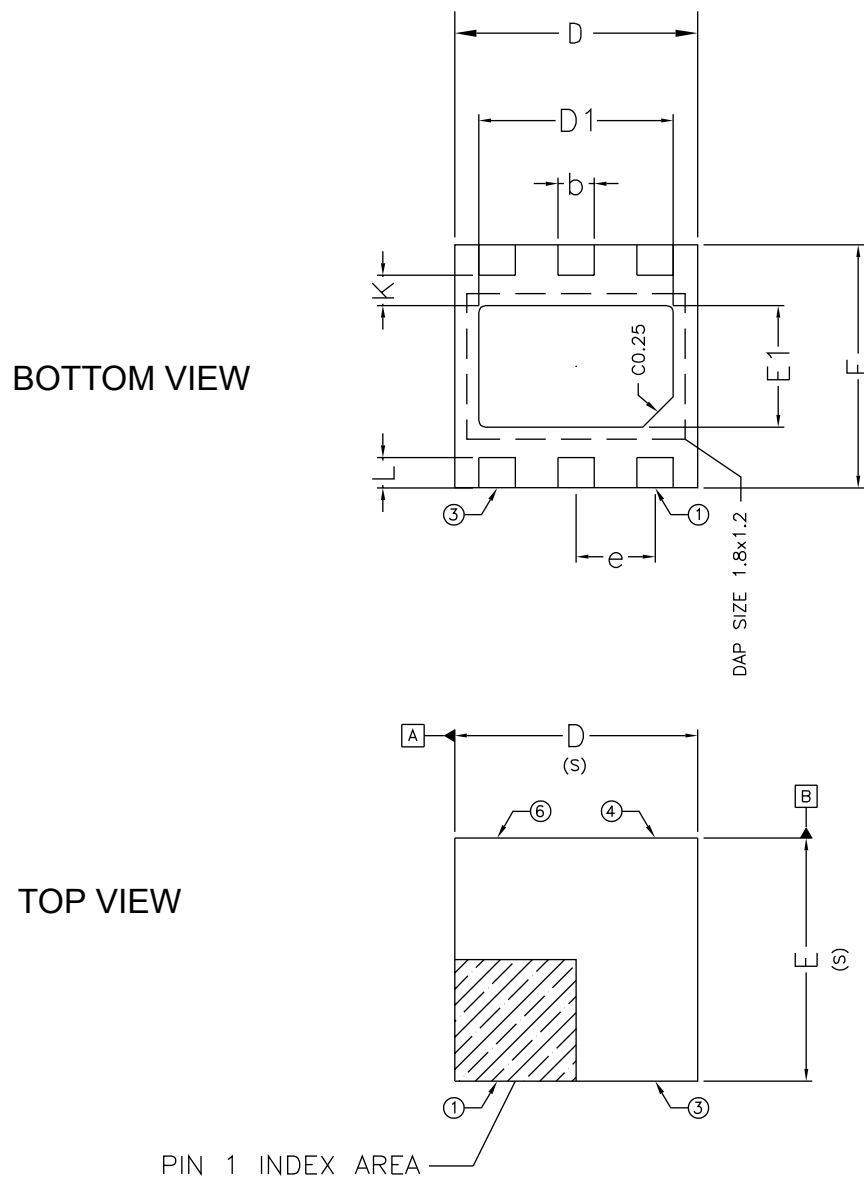


## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

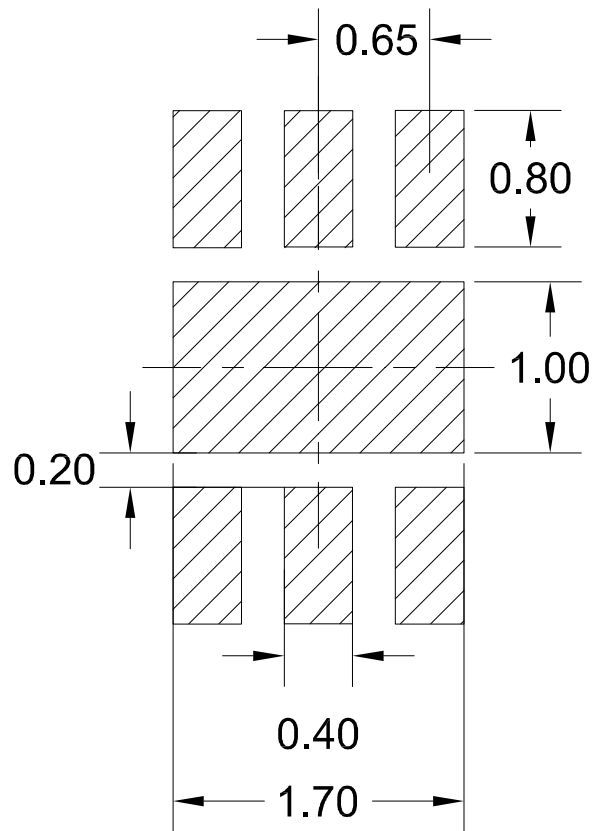
### 8.1 DFN6 (2 x 2) package information

Figure 26. DFN6 (2 x 2) package outline



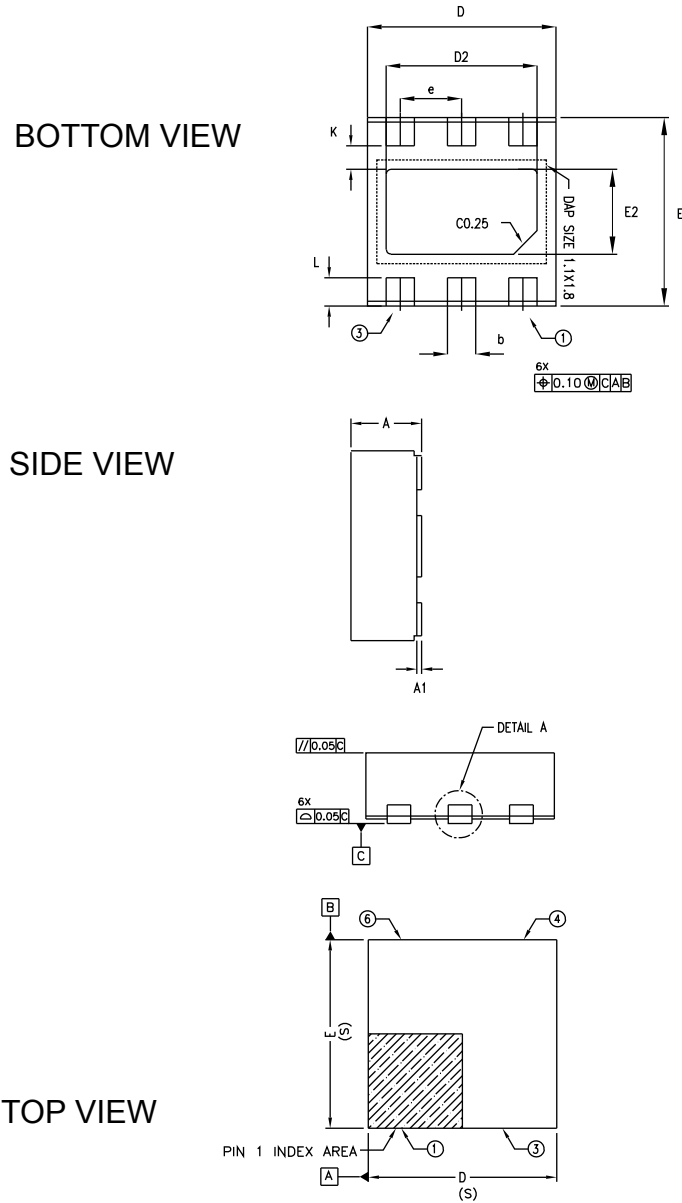
**Table 8. DFN6 (2 x 2) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00		0.05
A3	0.200 REF		
b	0.25	0.30	0.35
D	1.95	2.00	2.05
D1	1.50	1.60	1.70
e	0.65 BSC		
e2	0.25 REF		
E	1.95	2.00	2.05
E1	0.90	1.00	1.10
K		0.25	
L	0.15	0.25	0.35

**Figure 27. DFN6 (2 x 2) recommended footprint**


## 8.2 DFN6 (2 x 2) wettable flanks package information

Figure 28. DFN6 (2 x 2) wettable flanks package outline

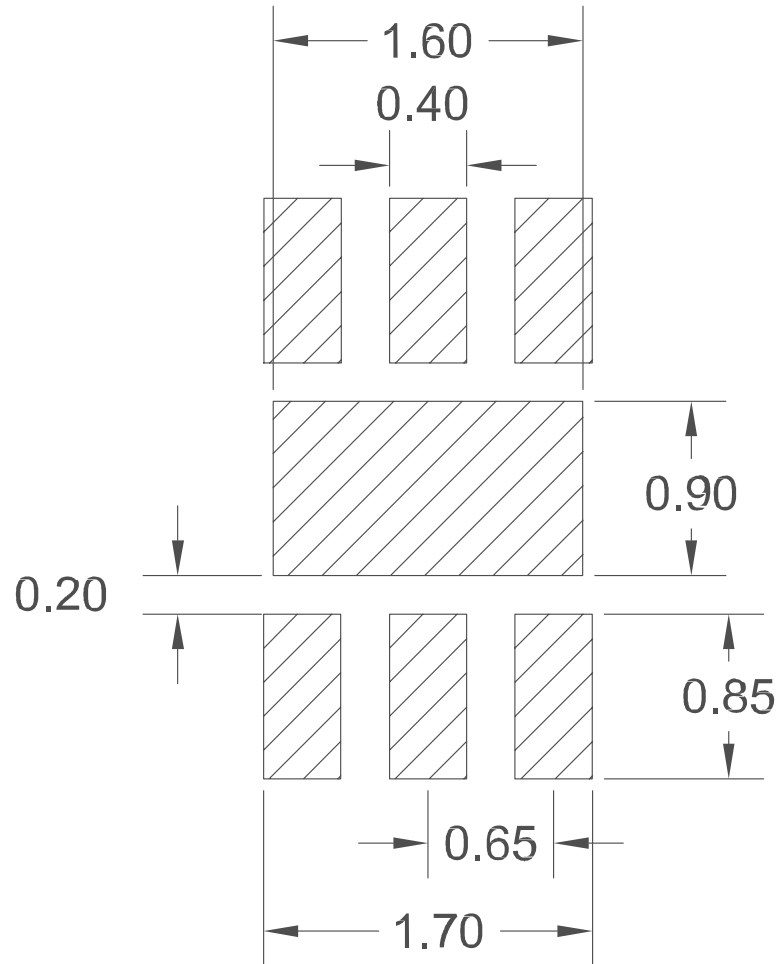




**Table 9. DFN6 (2 x 2) wettable flanks mechanical data**

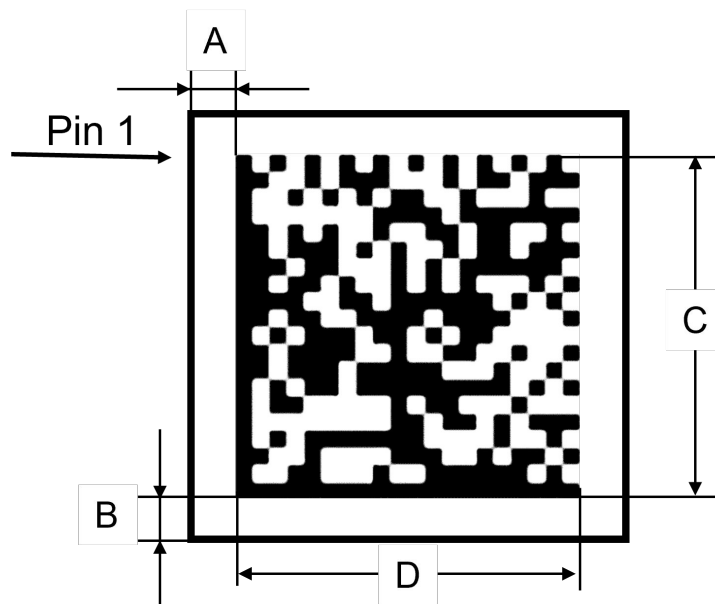
Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00		0.05
b	0.25	0.30	0.35
D	1.95	2.00	2.05
D2	1.50	1.60	1.70
e	0.65 BSC		
E	1.95	2.00	2.05
E2	0.80	0.90	1.00
L	0.20	0.30	0.40
K	0.25 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.10		

Figure 29. DFN6 (2 x 2) wettable flanks recommended footprint



### 8.3 DFN6 WF 2D marking information

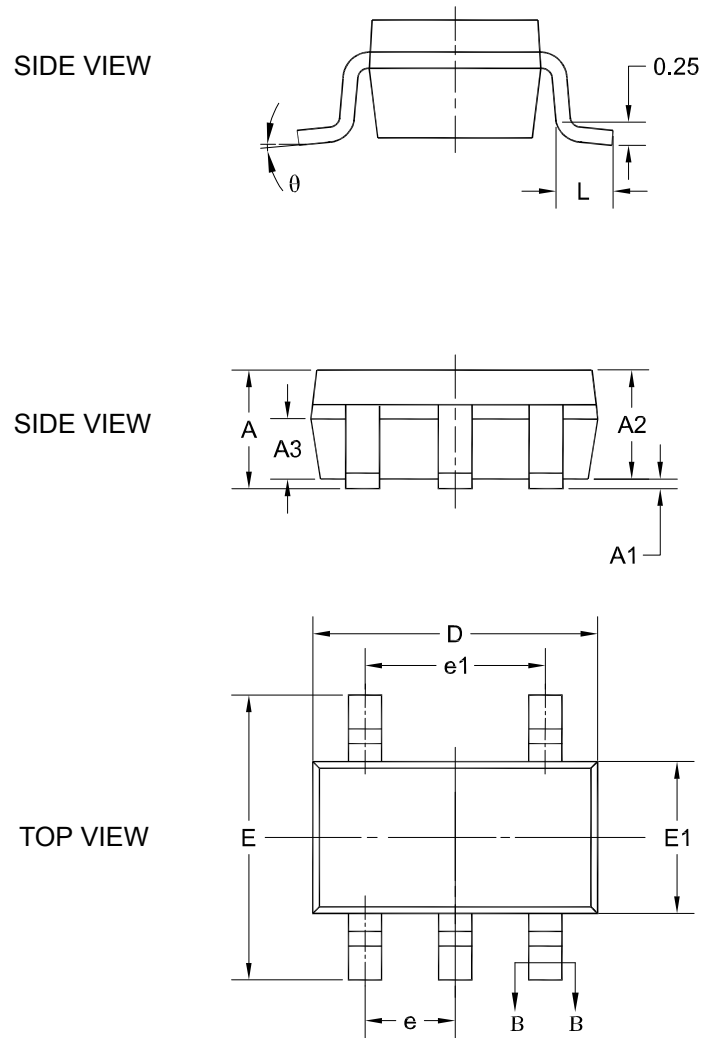
Figure 30. DFN6 WF 2D marking



Spec	UTL
A	0.2 mm
B	0.2 mm
C	1.6x1.6 (+/-0.125) mm.
D	1.6x1.6 (+/-0.125) mm.

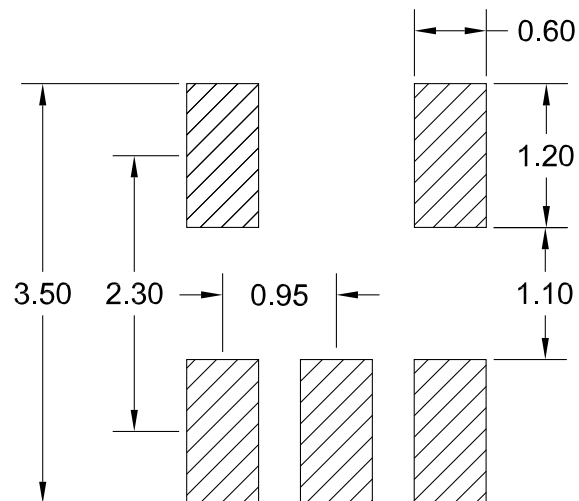
## 8.4 SOT23-5L package information

Figure 31. SOT23-5L package outline



**Table 10. SOT23-5L mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.25
A1	0.04		0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33		0.41
b1	0.32	0.35	0.38
c	0.15		0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 CS		
e1	1.90 BSC		
L	0.30		0.60
Θ	0		8°

**Figure 32. SOT23-5L recommended footprint**


## 9 DFN6 (2x2 mm) packing information

Figure 33. DFN6 (2x2 mm) tape outline

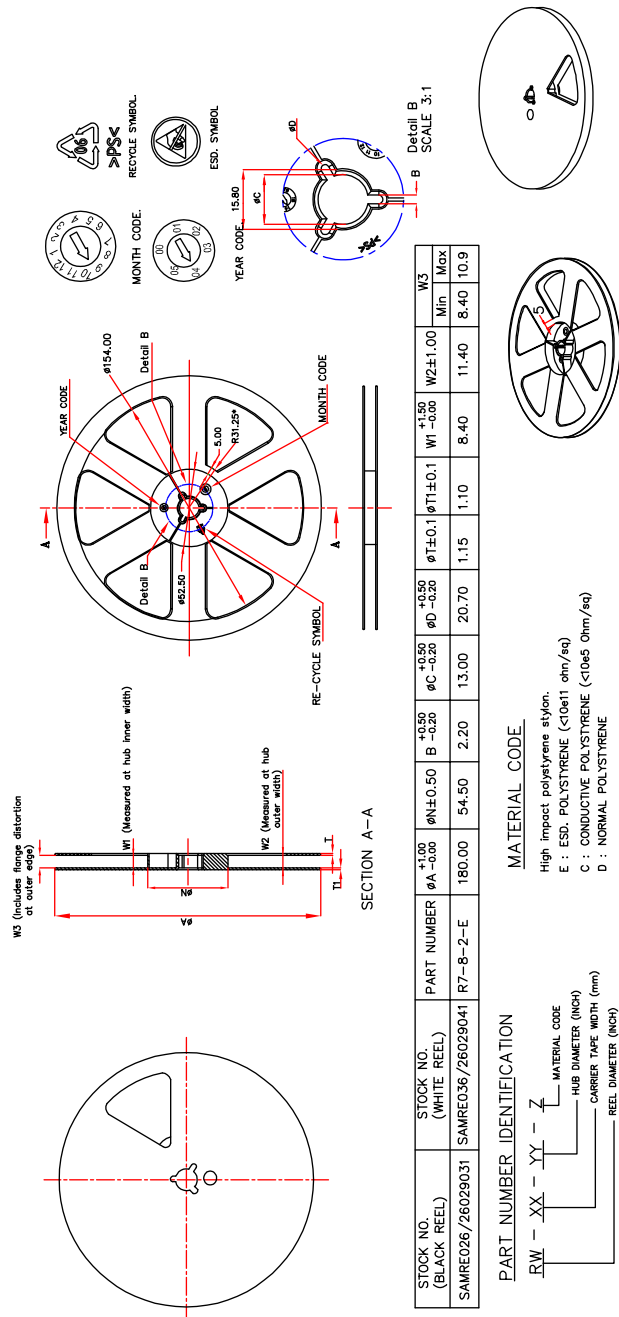


Figure 34. DFN6 (2x2 mm) reel outline

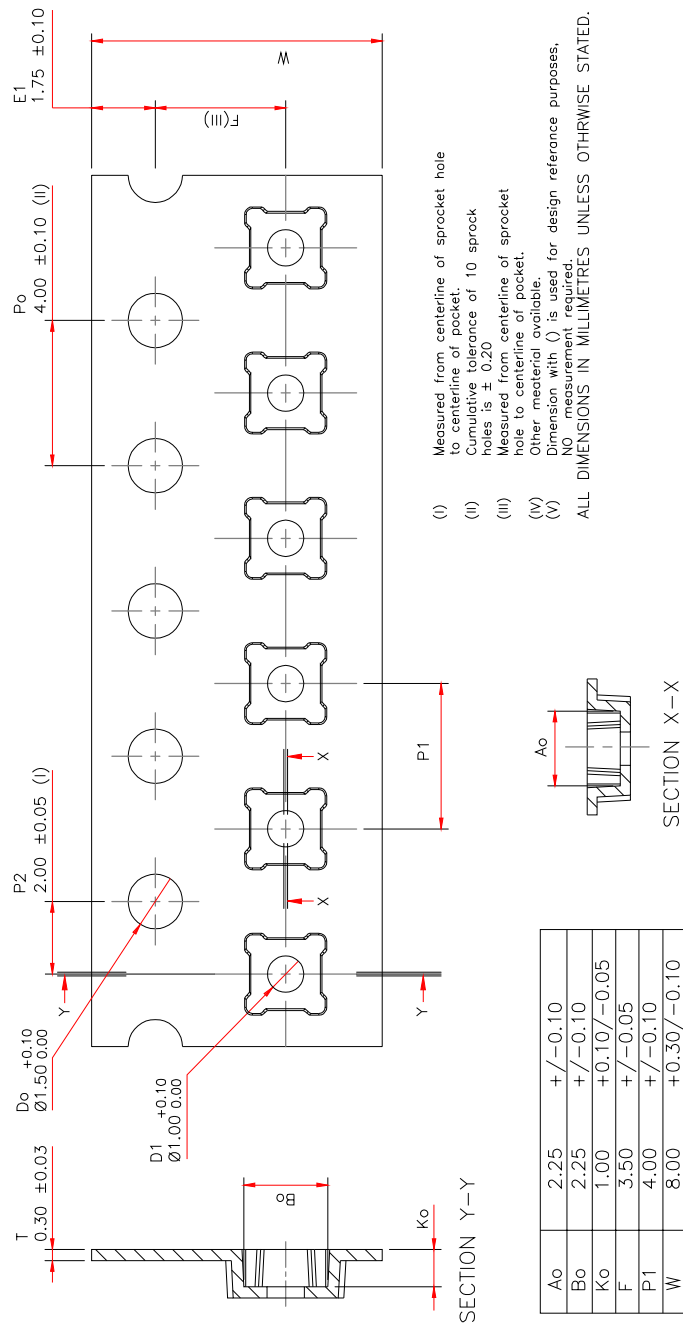


Figure 35. Pin 1 orientation

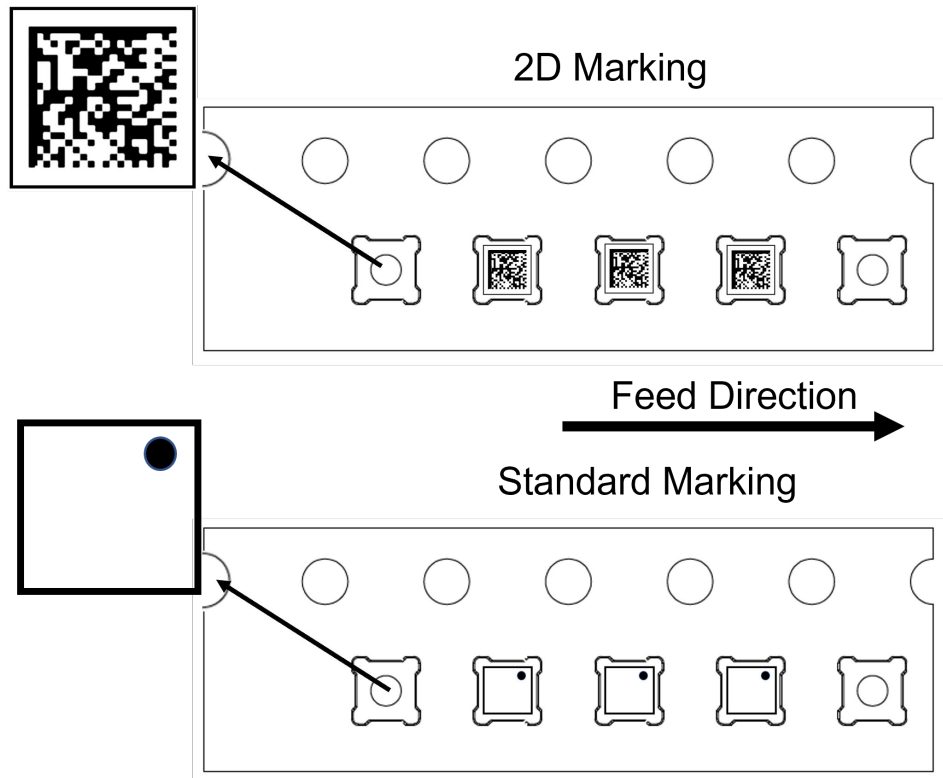
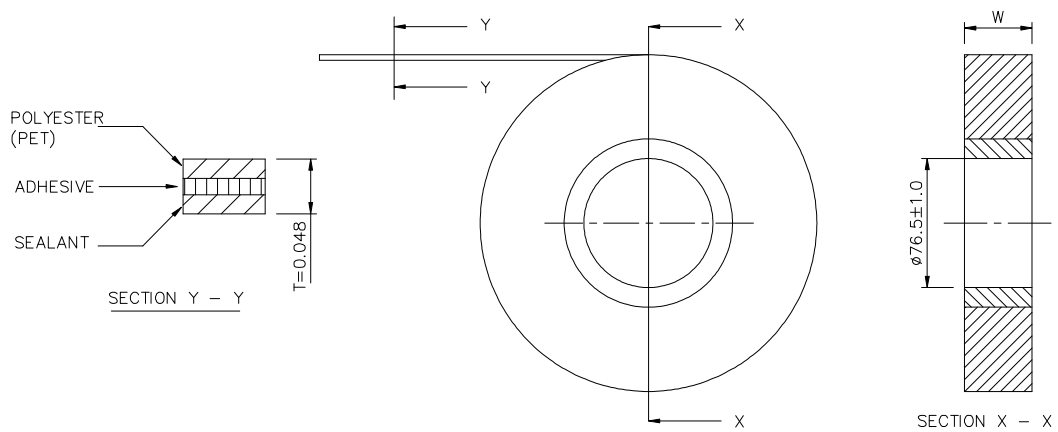


Figure 36. DFN6 (2x2 mm) cover tape outline



COVER TAPE WIDTH* ( W ±0.1 )	CARRIER TAPE WIDTH
5.3, 5.4, 5.5	8
9.2, 9.3, 9.5	12
13.3, 13.5	16
21.0, 21.3	24
25.5	32
37.5	44
49.5	56
81.5	88

NOTES

- 1 THICKNESS : 0.041 – 0.055
- 2 STANDARD LENGTH : 300m or 500m
- 3 TENSILE STRENGTH : >5.0kg/mm sq.
- 4 ELONGATION : >75%
- 5 SURFACE RESISTANCE: 1E+4 TO 9.9E+10 ohms.  
SURFACE RESISTIVITY: 1E+5 TO 9.9E+11 ohms/sq.
- 6 PEEL STRENGTH CONFORMS TO EIA SPEC: 20 TO 80g
- 7 RECOMMENDED SHELF LIFE : 2 YEARS  
FROM MANUFACTURING DATE
- 8 LUMINOUS TRANSMITTANCE : 87.8%
- 9 HAZE : 28%
- \*10 OTHER COVER TAPE WIDTH REFER TO WI4.08-04.



## 10 Ordering information

**Table 11. Order codes**

Order code	Package	V <sub>OUT</sub>	Marking
LDH40PURY <sup>(1)</sup>	DFN6 2x2 wettable flanks	ADJ	2D code
LDH40MR	SOT23 5L	ADJ	H40A
LDH40PUR <sup>(2)</sup>	DFN6 2x2	ADJ	

1. Automotive part according to AEC-Q100 Grade1
2. On request

## Revision history

**Table 12. Document revision history**

Date	Revision	Changes
18-Dec-2023	1	Initial release.
05-Mar-2024	2	Updated <a href="#">Table 7</a> , <a href="#">Figure 11</a> and <a href="#">Table 11</a> .

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