



MP2755

Bi-directional 2:1/1:2 Switched Cap Converter With Shipping Mode Function

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

MP2755 is a highly-integrated bi-directional charging solution for 2-cell Li-ion or Li-polymer batteries. It employs an inductor-less switched cap architecture, can provide up to 10A output current in forward mode and 5A charging current in reverse mode.

The MP2755 is suitable for applications migrating from 1-cell battery to 2-cell configuration. Combined with a 2-cell battery, it can be treated as a virtual 1-cell battery, allowing the existing downstream 1-cell power architecture to be compatible with 2-cell battery pack.

The MP2755 integrates shipping mode function which can shut down V1X output with minimum battery current consumption. It also support system reset function.

The I²C interface offers complete operating control, charging / discharging parameter programming and status monitoring.

The MP2755 is available in a WLCSP-42 (2.90mm x 2.55mm) package.

FEATURES

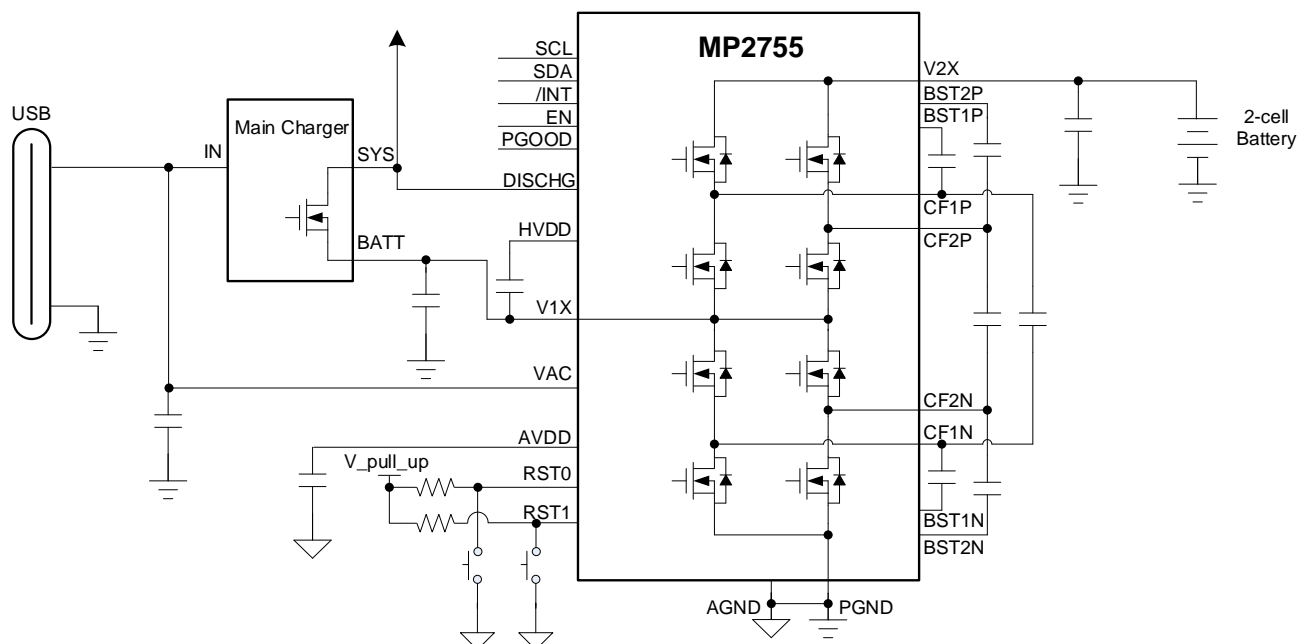
- Bi-directional switched capacitor converter
 - Forward 2:1 conversion
 - Reverse 1:2 conversion
- Dual-phase operation with 10A output current capability in forward direction
- 5A charge current capability in reverse direction
- Up to 99.3% efficiency
- Shipping mode and reset mode
- Audio mode to eliminate audible noise
- Dead battery activation power path

APPLICATIONS

- Smart phones
- Tablet PCs

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TYPICAL APPLICATION





MP2755 – BI-DIRECTIONAL SWITCHED CAP CONVERTER WITH SHIPPING MODE

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MP2755GC-xxxx**	WLCSP-42 (2.90mmx2.55mm)	See Below	1
EVKT-MP2755	Evaluation kit		

* For Tape & Reel, add suffix -Z (e.g. MP2755GC-xxxx-Z).

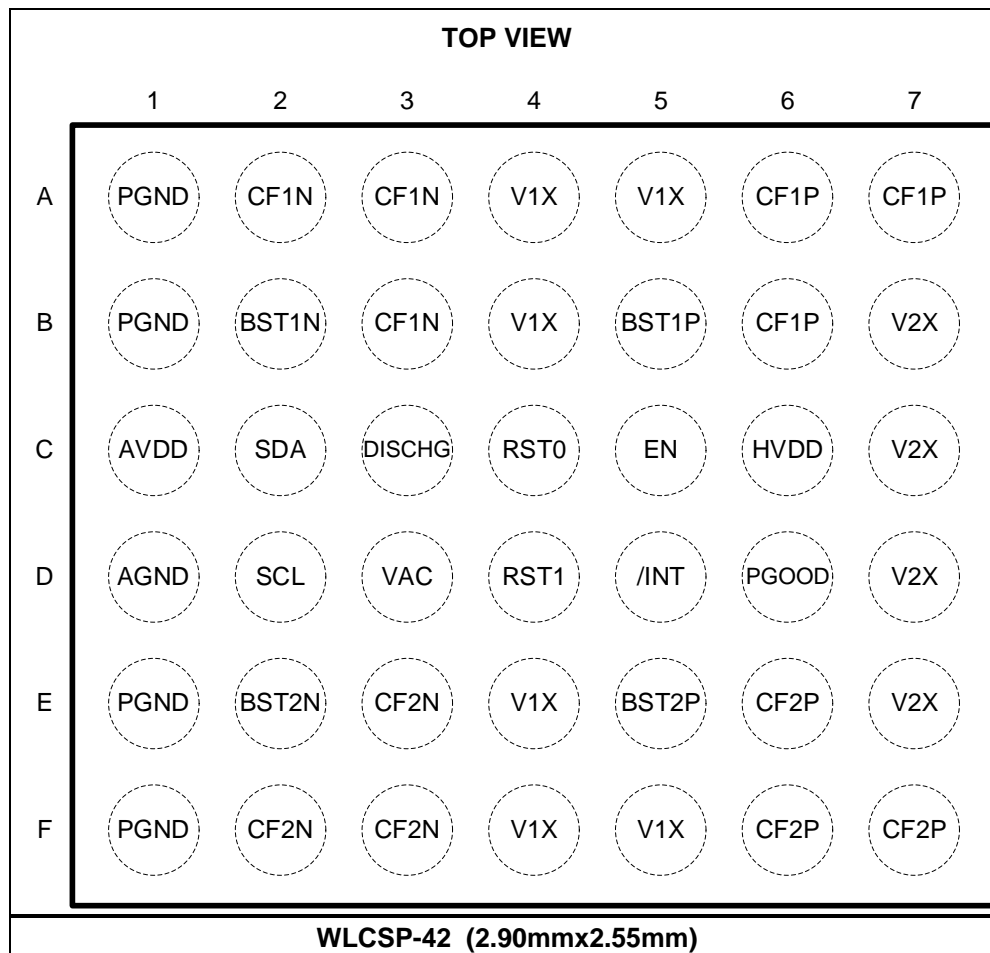
** "-xxxx" is the configuration code identifier for the register settings stored in the OTP register. Each "-x" can be a hexadecimal value between 0 and F. The default code is "-0000." Contact an MPS FAE to create this unique number.

*** Moisture Sensitivity Level Rating

TOP MARKING

(TBD)

PACKAGE REFERENCE





PIN FUNCTIONS

Pin #	Name	Type ⁽¹⁾	Description
A1, B1, E1, F1	PGND	P	Power ground.
A2, A3, B3	CF1N	P	Flying capacitor 1 negative terminal.
F2, E3, F3	CF2N	P	Flying capacitor 2 negative terminal.
A4, B4, A5, E4, F4, F5	V1X	P	Device power output.
A6, B6, A7	CF1P	P	Flying capacitor 1 positive terminal. Connect 3x47 μ F capacitor between CF1P and CF1N.
E7, F6, F7	CF2P	P	Flying capacitor 2 positive terminal. Connect 3x47 μ F capacitor between CF2P and CF2N.
B2, C2, D2, E2	V2X	P	Device power input.
C1	AVDD	AO	LDO output. Connect a 4.7 μ F capacitor between this pin and GND.
D1	AGND	AIO	Analog ground.
B2	BST1N	P	Bootstrap capacitor for phase 1. Connect a 100nF/10V ceramic capacitor from BST1N to CF1N.
E2	BST2N	P	Bootstrap capacitor for phase 2. Connect a 100nF/10V ceramic capacitor from BST2N to CF2N.
G7	SDA	DI	I ² C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10k Ω). The IC works as a slave.
F7	SCL	DIO	I ² C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10k Ω). The IC works as a slave.
C3	DISCHG	P	Discharge pin in reset mode.
D3	VAC	AI	Input voltage sense pin.
C4	RST0	DI	Reset input 0. Active low. Do not float RST0.
D4	RST1	DI	Reset input 1. Active low. Do not float RST1.
B5	BST1P	P	Bootstrap capacitor for phase 1. Connect a 100nF/10V ceramic capacitor from BST1P to CF1P.
C5	EN	DI	Enable pin.
D5	/INT	DO	Open drain, active low interrupt output. Pull up to a logic rail with 10k Ω resistor.
E5	BST2P	P	Bootstrap capacitor for phase 2. Connect a 100nF/10V ceramic capacitor from BST2P to CF2P.
C6	HVDD	AO	Bootstrap capacitor for both phase 1 and phase 2. Connect a 1 μ F/10V ceramic capacitor from HVDD to V1X.
D6	PGOOD	DO	Power good indicator output. High indicates the switched capacitor is switching.

(1) AI = Analog Input, AO = Analog Output, AIO = Analog Input Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input Output, P = Power

**ABSOLUTE MAXIMUM RATINGS** ⁽¹⁾

VAC to PGND	-0.3V to +28V
V2X to PGND.....	-0.3V to +16V
V1X, DISCHG to PGND.....	-0.3V to +6V
CF1P, CF2P to PGND	-0.3V to +12V
CF1P, CF2P to V1X.....	-0.3V to +6V
CF1N, CF2N to PGND.....	-0.3V to +6V
HVDD to PGND	-0.3V to +11V
BST1P to CF1P, BST2P to CF2P ...	-0.3V to +5V
BST1N to CF1N, BST2N to CF2N ..	-0.3V to +5V
HVDD to V1X.....	-0.3V to +5V
EN to AGND	-0.3V to +16V
RST0, RST1 to AGND	-0.3V to +6V
All Other Pins to AGND.....	-0.3V to +5V
Continuous power dissipation ($T_A = 25^\circ\text{C}$) ⁽²⁾	TBD
Junction temperature	150°C
Lead temperature (solder)	260°C
Storage temperature	-65°C to +150°C

ESD Ratings

Human body model (HBM) ⁽³⁾	2000V
Charged device model (CDM) ⁽⁴⁾	750V

Recommended Operating Conditions ⁽⁵⁾

Supply voltage (V_{VAC}).....	Up to 20V
V1X voltage (V_{OUT}).....	Up to 5.5V
V2X voltage (V_{OUT}).....	Up to 11V
Operating junction temp (T_J)....	-40°C to +125°C

Thermal Resistance ⁽⁶⁾ θ_{JA} θ_{JC}

WLCSP42 (2.90mm x 2.55mm)

..... TBD ... TBD . °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Per ANSI/ESDA/JEDEC JS-001, all pins.
- 4) Per ANSI/ESDA/JEDEC JS-002, all pins.
- 5) The device is not guaranteed to function outside of its operating conditions.
- 6) Measured on JESD51-7, 4-layer PCB.

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