

# **MP6590** 80V High-Side MOSFET Driver

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

## DESCRIPTON

The MP6590 is a driver for a high-side Nchannel power MOSFET. It generates a gate drive voltage above the input supply to drive an N-channel gate. It can source and sink 1A of current to quickly enable and disable large power MOSFETs. The MP6590 can operate on supply voltages up to 80V.

Internal safety features include undervoltage lockout (UVLO), and thermal shutdown.

The MP6590 is available in a 3mm x 4mm FCQFN package with wettable flanks.

A low voltage (LV) version, with lower gate drive voltage and UVLO, is available on special order.

## FEATURES

- 7.5V to 80V Operating Input Voltage Range
- Gate Drive Charge Pump Generates Voltage 12V Above Input
- Thermal Shutdown
- Undervoltage Lockout
- Low-power Sleep Mode (<1µA)</li>
- Fault Indication Output
- FCQFN(3mmx4mm) Package

## APPLICATIONS

- Battery Power Tools
- Automotive High-Side Switches

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## **TYPICAL APPLICATION**





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## **ORDERING INFORMATION**

Part Number*	Package	Top Marking	MSL Rating	
MP6590GLE	QFN (3mmx4mm) (wettable flank)	See Below	1	

\* For Tape & Reel, add suffix -Z (e.g. MP6590GLE-Z);

## **TOP MARKING**

(TBD)





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## **PIN FUNCTIONS**

Pin #	Name	Description
7	ON	Input pin. High drives G to VIN + 12V; Low drives G to VOUT. Internal pull down resistor.
8	ENBL	Enable input. Low powers down device and drives G to VOUT. Internal pull down resistor.
6	nFAULT	Fault Indication. Open-drain output, logic low when in fault condition (OTP or UVLO).
2	VOUT	Connect to MOSFET source (switch output).
3	G	Connect to MOSFET gate.
5	BST	Gate drive power supply. Connect to a 100nF capacitor rated for at least 16V to VCP. See text.
4	VCP	Charge pump output. Connect to a 100nF capacitor rated for at least 16V to BST. See text.
1	VIN	Input Supply Voltage. Decouple to GND with minimum 100nF ceramic capacitor to GND. Additional bulk capacitance may be desirable.
9	RSVD	Reserved. Do not connect this pin.
10, 11	GND	System ground connection.

## **ABSOLUTE MAXIMUM RATINGS** (1)

Supply Voltage V <sub>IN</sub> VOUT, G Voltage	0.3V to 100V 2V to 100V
VCP Voltage	0.7V to 100V
BST Voltage	0.7V to 100V
VOUT-G Voltage	0.7V to 20V
All Other Pins to GND	0.3V to 6.5V
Continuous Power Dissipation	(T <sub>A</sub> = +25°C) <sup>(2)</sup>
	TBDW
Storage Temperature	-55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Solder)	+260°C

#### ESD Rating

Human-body model (HBM) ...... 2000V<sup>(4)</sup> Charged Device Model (CDM)......750V<sup>(5)</sup>

#### **Recommended Operating Conditions**

Supply Voltage  $V_{IN}$  (MP6590) .......7.5V to 80V Supply Voltage  $V_{IN}$  (LV version) .....4.5V to 80V Operating Junction Temp. (T<sub>J</sub>). -40°C to +150°C

## Thermal Resistance <sup>(3)</sup> θ<sub>JA</sub> θ<sub>JC</sub>

QFN (3mmx4mm).....TBD...TBD...°C/W

#### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-toambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX)-T<sub>A</sub>)/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Measured on JESD51-7, 4-layer PCB.
- 4) Per AECQ100-002
- 5) Per AECQ100-011



#### PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

## **ELECTRICAL CHARACTERISTICS**

 $V_{IN}$  = 14V,  $T_A$  = -40 to +150°C, unless otherwise noted.

Power Supply         VIN         MP6590         7.5         80         V           Input Supply Voltage $V_{IN}$ MP6590         7.5         80         V           Quiescent Current         I <sub>Q</sub> No load current, ENBL = 1         1.3         1.5         mA           Gate Drive Output         Shutdown mode, ENBL = 0         2 $\mu$ A           Gate Drive Output         Rpp         400 $\Omega$ $\Omega$ Output On Resistance         Rpp         10 $\Omega$ $\Omega$ Peak Output Current         Iourp         1         A         A           Input Logic 'Low' Threshold         ViL         1         A         A           Input Logic 'Low' Threshold         ViL         0.8         V           Input Logic 'Low' Threshold         ViL         2         V         V           Logic Input Current         Inv(L)         ViL=5V         -20         20 $\mu$ A           Internal Pull Down Resistance         Rpp         Io=5mA         0.5         V         V           Output Low Voltage         VoL         Io=5mA         1 $\mu$ A         V           UPLO Rising Threshold         VuV         Io=5	Parameter	Symbol	Condition Min Typ			Max	Units		
$ \begin{array}{ c c c c c c } \mbox{Input Supply Voltage} & V_{\rm IN} & \frac{MP6590}{LV Version (metal option)} & 4.5 & 80 \\ \hline Version (metal option) & 4.5 & 80 \\ \hline VVersion (metal option) & 3.7 & 4 & 4.3 \\ \hline VVersion (metal option) & 3.7 & 4 & 4.3 \\ \hline VVLO Rising Threshold & V_{UV} & MP6590 & 6.6 & 7 & 7.4 \\ \hline VVLO Rising Threshold & V_{UV} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VVP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VVP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VVP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & MP6590 & 5.8 & 6.5 & 7.2 \\ \hline VP Threshold Voltage & V_{VVFM} & VVF & VVF & VVF & VVF & VVF & VVF $	Power Supply								
$\begin{array}{ c c c c c c } \mbox{Higher} & ViN & LV Version (metal option) & 4.5 & 80 & V \\ \hline \mbox{Higher} & ViN & LV Version (metal option) & 4.5 & 80 & V \\ \hline \mbox{Higher} & No load current, ENBL = 1 & 1.3 & 1.5 & mA \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 2 & \muA \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 2 & \muA \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 2 & \muA \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 10 & \Omega \\ \mbox{Jack Schuld own mode, ENBL = 0 & 10 & \Omega \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 10 & \Omega \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 10 & \Omega \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 10 & \Omega \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 10 & \Omega \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 10 & \Omega \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own mode, ENBL = 0 & 11 & A \\ \hline \mbox{Jack Schuld own Threshold Vit} & V_{IL & Iourp High Logic 'Low' Threshold Vit & V_{IL & Iourp High Logic 'Low' Threshold Vit & V_{IL & Iourp High Leakage Current I & Iourp V \\ \hline \mbox{Jack Schuld own Voltage Voltage Volt Io=SmA & 0.5 V & 0 \\ \hline \mbox{Jack Schuld Woltage Voltage Volt MP6590 & 6.6 & 7 & 7.4 \\ \hline \mbox{Jack Schuld Voltage Voltage Voltage Nucleon (metal option) & 3.7 & 4 & 4.3 & V \\ \hline \mbox{Jack Schuld Woltage Voltage Voltage Nucleon (metal option) & 3.7 & 4 & 4.3 & V \\ \hline \mbox{Jack Schuld Woltage Voltage Nucleon (metal option) & 2.6 & 3 & 3.4 & V \\ \hline \mbox{Jack Schuld Woltage Voltage Voltage Nucleon (metal option) & 2.6 & 3 & 3.4 & V \\ \hline \mbox{Thermal Shutdown Hysteresis ATrso Voltage Vin + Vin + Vin + } \\ \hline \mbox{Jack Schuld Woltage Vin + Vin + Vin + Vin + } \\ \hline Jack Schuld Woltage Vin + Vin + Vi$	Input Supply Voltage	Mar	MP6590	7.5		80	V		
		V IN	LV Version (metal option)	4.5		80			
		Ι <sub>Q</sub>	No load current, ENBL = 1		1.3	1.5	mA		
$\begin{tabular}{ c c c c } \hline Gate Drive Output On Resistance & $$R_{PU}$ & $$A00$ & $$\Omega$ & $	Quiescent Current	I <sub>SHDN</sub>	Shutdown mode, ENBL = 0 25°C			2	μA		
$\begin{array}{c c c c c c c } Output On Resistance & \hline R_{PU} & & & & & & & & & & & & & & & & & & &$	Gate Drive Output								
$\begin{tabular}{ c c c c c c } \hline $R_{PD}$ & 10 & $\Omega$ \\ \hline $Peak Output Current$ & $louTP$ & $1$ & $A$ \\ \hline $louTP$ & $1$ & $1$ & $A$ \\ \hline $IouTP$ & $1$ & $1$ & $A$ \\ \hline $IouTP$ & $1$ & $1$ & $A$ \\ \hline $IouTP$ & $1$ & $1$ & $A$ \\ \hline $IouTP$ & $1$ & $1$ & $A$ \\ \hline $IouTP$ & $1$ & $1$ & $1$ & $A$ \\ \hline $IouTP$ & $1$ & $1$ & $1$ & $A$ \\ \hline $IouTP$ & $1$ & $1$ & $1$ & $A$ \\ \hline $IouTP$ & $1$ & $1$ & $1$ & $A$ \\ \hline $Input Logic 'Low' Threshold & $V_{IL}$ & $1$ & $0$ & $8$ & $V$ \\ \hline $Input Logic 'High' Threshold & $V_{IL}$ & $1$ & $1$ & $0$ & $8$ & $V$ \\ \hline $Input Logic 'High' Threshold & $V_{IH}$ & $1$ & $1$ & $1$ & $0$ & $1$ & $$	Output On Registeres	R <sub>PU</sub>			400		Ω		
$\begin{array}{c c c c c c } \hline Peak Output Current & lourp & 1 & A \\ \hline lourp & 1 & A \\ \hline lourp & 1 & A \\ \hline \hline control Logic \\ \hline Input Logic 'Low' Threshold & V_{IL} & 0.8 & V \\ \hline Input Logic 'High' Threshold & V_{IH} & 2 & 0.8 & V \\ \hline Input Logic 'High' Threshold & V_{IH} & 2 & V \\ \hline Logic Input Current & Inv(H) & V_{IH}=5V & -20 & 20 & \muA \\ \hline Internal Pull Down Resistance & R_{PD} & 500 & k\Omega \\ \hline nFault Output (Open-Drain Output) \\ \hline Output Low Voltage & V_{OL} & I_{O}=5mA & 0.5 & V \\ Output Low Voltage & V_{OL} & I_{O}=5mA & 0.5 & V \\ Output High Leakage Current & I_{OH} & V_{O}=3.3V & -2 & 1 & \muA \\ \hline Protection Circuits & & & & & & & & & & & & & \\ \hline UVLO Rising Threshold & V_{UV} & MP6590 & 6.6 & 7 & 7.4 & V \\ UVLO Blanking Time & tvB & From ON=1 & 20 & \muS \\ \hline VCP Threshold Voltage & V_{VCPMIN} & MP6590 & 5.8 & 6.5 & 7.2 & V \\ \hline Dversion (metal option) & 2.6 & 3 & 3.4 & V \\ \hline Thermal Shutdown Hysteresis & \Delta T_{TSD} & 180 & ^{\circ}C \\ \hline Thermal Shutdown Hysteresis & \Delta T_{TSD} & 25 & ^{\circ}C \\ \hline MP6590 & VIN + & VIN + & VIN + \\ \hline \end{array}$		R <sub>PD</sub>			10		Ω		
$\begin{array}{c c c c c c } \hline Preak Output Current & lourp & 1 & A \\ \hline \mbox{Control Logic} & & & & & & & & & & & & & & & & & & &$	Reak Output Current	IOUTP			1		А		
$\begin{tabular}{ c c c } \hline Control Logic \\ \hline Input Logic 'Low' Threshold & V_{IL} & & & & & & & & & & & & & & & & & & &$		IOUTP			1		А		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Control Logic	r	1	T	T				
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Logic 'Low' Threshold	VIL				0.8	V		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Logic 'High' Threshold	VIH		2			V		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Logic Input Current	IIN(H)	VIH=5V	-20		20	μA		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		I <sub>IN(L)</sub>	VIL=0.8V	-20		20	μA		
$\begin{array}{ c c c c c c c } \hline \text{NFault Output (Open-Drain Output)} \\ \hline Output Low Voltage & V_{OL} & I_O=5mA & & & 0.5 & V \\ \hline Output High Leakage Current & I_{OH} & V_O=3.3V & & & 1 & \muA \\ \hline \textbf{Protection Circuits} \\ \hline UVLO Rising Threshold & V_{UV} & MP6590 & 6.6 & 7 & 7.4 & V \\ \hline UVLO Hysteresis & \Delta V_{UV} & & & 500 & mV \\ \hline UVLO Hysteresis & \Delta V_{UV} & & & 500 & mV \\ \hline UVLO Blanking Time & t_{UVB} & From ON=1 & 20 & \muS \\ \hline VCP Threshold Voltage & V_{VCPMIN} & MP6590 & 5.8 & 6.5 & 7.2 & V \\ \hline LV version (metal option) & 2.6 & 3 & 3.4 & V \\ \hline Thermal Shutdown & T_{TSD} & & & 180 & ^{\circ}C \\ \hline Thermal Shutdown Hysteresis & \Delta T_{TSD} & & & & 25 & ^{\circ}C \\ \hline \textbf{Charge Pump} & & & & & & & & \\ \hline \ MP6590 & VIN + & VIN + & VIN + & & & \\ \hline \end{array}$	Internal Pull Down Resistance R <sub>PD</sub>				500		kΩ		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	nFault Output (Open-Drain Out	tput)							
$\begin{array}{c c c c c c c c } \hline Output High Leakage Current & I_{OH} & V_0=3.3V & & & & 1 & \muA \\ \hline Protection Circuits & & & & & \\ \hline UVLO Rising Threshold & V_{UV} & \underline{MP6590} & 6.6 & 7 & 7.4 & V \\ \hline UVLO Rising Threshold & V_{UV} & \underline{LV \ version \ (metal \ option)} & 3.7 & 4 & 4.3 & V \\ \hline UVLO Hysteresis & \Delta V_{UV} & & & & 500 & & mV \\ \hline UVLO Blanking Time & t_{UVB} & From \ ON=1 & 20 & & \muS \\ \hline VCP \ Threshold \ Voltage & V_{VCPMIN} & \underline{MP6590} & 5.8 & 6.5 & 7.2 & V \\ \hline LV \ version \ (metal \ option) & 2.6 & 3 & 3.4 & V \\ \hline Thermal \ Shutdown \ Hysteresis & \Delta T_{TSD} & & & & 180 & ^{\circ}C \\ \hline Thermal \ Shutdown \ Hysteresis & \Delta T_{TSD} & & & & & & 25 & & ^{\circ}C \\ \hline Charge \ Pump & & & & & & & & & \\ \hline MP6590 & VIN \ + & VIN \ + & VIN \ + & VIN \ + & & & & \\ \hline \end{array}$	Output Low Voltage	Vol	Io=5mA			0.5	V		
$\begin{tabular}{ c c c c } \hline Protection Circuits \\ \hline UVLO Rising Threshold & V_{UV} & MP6590 & 6.6 & 7 & 7.4 & V \\ \hline UVLO Hysteresis & \Delta V_{UV} & LV version (metal option) & 3.7 & 4 & 4.3 & \\ \hline UVLO Hysteresis & \Delta V_{UV} & rom ON=1 & 20 & \muS \\ \hline UVLO Blanking Time & t_{UVB} & From ON=1 & 20 & \muS \\ \hline VCP Threshold Voltage & V_{VCPMIN} & MP6590 & 5.8 & 6.5 & 7.2 & V \\ \hline LV version (metal option) & 2.6 & 3 & 3.4 & \\ \hline Thermal Shutdown Hysteresis & \Delta T_{TSD} & LV version (metal option) & 2.5 & 0 & °C \\ \hline Charge Pump & MP6590 & VIN + VIN + VIN + VIN + \\ \hline \end{tabular}$	Output High Leakage Current	I <sub>ОН</sub>	V <sub>0</sub> =3.3V			1	μA		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Protection Circuits	-							
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		Vinz	MP6590	6.6	7	7.4	V		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		• 00	LV version (metal option)	3.7	4	4.3	v		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	UVLO Hysteresis	$\Delta V_{UV}$			500		mV		
VCP Threshold Voltage         MP6590         5.8         6.5         7.2         V           Thermal Shutdown         T <sub>TSD</sub> LV version (metal option)         2.6         3         3.4         °C           Thermal Shutdown Hysteresis         ΔT <sub>TSD</sub> Image: Comparison of the state of the st	UVLO Blanking Time	tuvв	From ON=1		20		μS		
VCP Threshold Voltage         VCPMIN         LV version (metal option)         2.6         3         3.4         V           Thermal Shutdown         T <sub>TSD</sub> 180         °C           Thermal Shutdown Hysteresis         ΔT <sub>TSD</sub> 25         °C           Charge Pump         MP6590         VIN +         VIN +         VIN +	VCP Threshold Voltage	V	MP6590	5.8	6.5	7.2	V		
Thermal Shutdown         T <sub>TSD</sub> 180         °C           Thermal Shutdown Hysteresis         ΔT <sub>TSD</sub> 25         °C           Charge Pump         VIN +         VIN +         VIN +		VCPMIN	LV version (metal option)	2.6	3	3.4	V		
Thermal Shutdown Hysteresis         ΔT <sub>TSD</sub> 25         °C           Charge Pump         VIN +         VIN +         VIN +	Thermal Shutdown	T <sub>TSD</sub>			180		°C		
Charge Pump         VIN +         VIN +         VIN +	Thermal Shutdown Hysteresis	$\Delta T_{TSD}$			25		°C		
MP6590 VIN + VIN + VIN +	Charge Pump								
			MP6590	VIN +	VIN +	VIN +			
Gate Drive Output Voltage V <sub>CP</sub>	Gate Drive Output Voltage	V <sub>CP</sub>		10.5	12	13.5	V		
LV version (metal option) $4.5$ 5 6			LV version (metal option)	4.5	5	6			



PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

## TIMING CHARACTERISTICS

 $V_{\text{IN}}$  = 14V,  $T_{\text{A}}$  = -40 to +150°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Мах	Units
Enable Time	twake	From ENBL = Low to High		50		μS
Disable Time	t <sub>SLEEP</sub>	From ENBL = High to Low		200		nS
Power-up Time	t <sub>PUP</sub>	From V <sub>VCP</sub> > V <sub>VCPMIN</sub>		200		nS
Propagation Delay	t <sub>PD</sub>	IN to G=10V, C <sub>L</sub> = 10nF		200		nS



### PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

## **TYPICAL PERFORMANCE CHARACTERISTICS**

ON = 5V, EN = 5V,  $T_A = 25^{\circ}C$ , unless otherwise noted.





#### CH1: ON CH2: OUT CH4: IOUT CH4: IOUT CH3: G CH4: IOUT CH4: IOUT

#### Turn off the MOSFET







#### PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

## **TYPICAL PERFORMANCE CHARACTERISTICS** (continued)

ON = 5V, EN = 5V,  $T_A = 25^{\circ}C$ , unless otherwise noted.





PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

## **BLOCK DIAGRAM**



Figure 1: Functional Block Diagram



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## **OPERATION**

The MP6590, in combination with an external N-channel power MOSFET, is used to implement a high side switch. It generates the required gate drive voltage to fully enhance the external MOSFET, and provides control and protection functions.

#### Power-up

The MP6590 will start power-up when the VCP voltage exceeds  $V_{VCPMIN}$  and the ENBL pin is logic high. Turn-on of the external MOSFET is not allowed until VIN has exceeded the UVLO threshold  $V_{UVLO}$ , and the voltage at VCP has exceeded the  $V_{VCPMIN}$  threshold. There is a minimum delay of t<sub>PUP</sub> before the MOSFET can be enabled to prevent rapid cycling in a fault condition.

#### Input Logic

The MP6590 has two input pins: ON and ENBL. Both pins have internal pulldowns.

The ENBL pin enables and disables the part. When ENBL is logic low, the internal charge pump is disabled and internal circuitry is put into a low power state. The G pin is pulled to VOUT to keep the external MOSFET disabled.

When ENBL is taken to logic high, the part is enabled and the charge pump runs.

The ON pin is used to turn the external MOSFET on. Logic high drives the G pin to VIN+12V (MP6590) or VIN+5V (LV version metal option) to turn the MOSFET on. Logic low drives G to VOUT to turn the MOSFET off.

#### Charge Pump / Bootstrap

An external capacitor is used as a bootstrap to initially turn on the external MOSFET. Once the MOSFET is on, a weak charge pump is used to overcome leakages to allow 100% duty cycle operation indefinitely.

Note that there must be some load at the OUT pin (MOSFET source) to return the current needed (approximately 10uA) to charge the bootstrap capacitor when the MOSFET is turned off. The load resistance must be less than (VIN-6.5V) / 10uA. This equates to  $750k\Omega$  at a VIN voltage of 14V.

The gate drive voltage is regulated at a nominal 12V for the standard MP6590. The LV version (metal option) lowers this voltage to 5V.

If the charge pump voltage drops to below the charge pump threshold voltage  $V_{VCPMIN}$ , the external MOSFET will be turned off.

#### Gate Driver

N- and P-channel FETs are used to drive the gate of the external MOSFET to either the charge pump voltage, or to the output, which is the source terminal of the external MOSFET.

A protective diode needs to be placed at VOUT pin to prevent the negative voltage which generated when the external MOSFET turn-off from damaging the MP6590.

#### VIN UVLO Protection

If at any time the voltage on the VIN pin falls below the under-voltage lockout threshold, the external MOSFET will be turned off, and the device will turn off most internal circuitry and enter a low power state. Operation will resume when VIN rises above the UVLO threshold.

UVLO protection is disabled for a short time  $t_{\text{UVB}}$  after the external MOSFET is turned on.

#### **Overtemperature Protection**

If the die temperature exceeds safe limits, the G pin will be driven to VOUT to turn the MOSFET off, and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

#### nFAULT Output

MP6590 provides an nFAULT pin which is driven active low if any of the protection circuits are activated. These fault conditions include a VCP undervoltage, VIN undervoltage, and overtemperature. nFAULT is an open-drain output and requires an external pullup resistor. When the fault condition is removed, the nFAULT pin is pulled inactive high by the pullup resistor.

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## **APPLICATION INFORMATION**

#### **PCB Layout Guidelines**

Proper PCB layout is critical to the performance of high-side gate driver. For the best results, refer to Figure 2 and follow the guidelines below:

1. Make the connection between the OUT pin and the MOSFET source as direct as possible to avoid excessive undershoot on the OUT due to inductive load or parasitic inductance.

2. Place the  $C_{\text{BST}}$  and supply bypass capacitors as close as possible to the IC.

3. Use wide copper areas for all the high current paths.



Figure 2



PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

## **PACKAGE INFORMATION**

QFN 3mmx4mm (wettable flank)



TOP VIEW





#### BOTTOM VIEW





#### **RECOMMENDED LAND PATTERN**

#### NOTE:

1) THE LEAD SIDE IS WETTABLE.

2) ALL DIMENSIONS ARE IN MILLIMETERS.

- 3) LEAD COPLANARITY SHALL BE 0.08
- MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.



PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

## **CARRIER INFORMATION**





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6590GLE-Z	QFN (3mmx4mm) (wettable flank)	5000	N/A	N/A	13 in.	12 mm	8 mm

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