MP6590

80V High-Side MOSFET Driver

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTON

The MP6590 is a driver for a high-side N-channel power MOSFET. It generates a gate drive voltage above the input supply to drive an N-channel gate. It can source and sink 1A of current to quickly enable and disable large power MOSFETs. The MP6590 can operate on supply voltages up to 80V.

Internal safety features include undervoltage lockout (UVLO), and thermal shutdown.

The MP6590 is available in a 3mm x 4mm FCQFN package with wettable flanks.

A low voltage (LV) version, with lower gate drive voltage and UVLO, is available on special order.

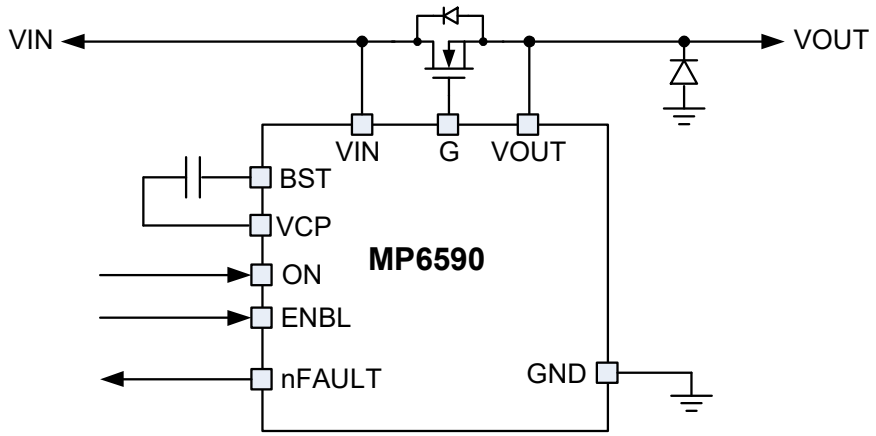
FEATURES

- 7.5V to 80V Operating Input Voltage Range
- Gate Drive Charge Pump Generates Voltage 12V Above Input
- Thermal Shutdown
- Undervoltage Lockout
- Low-power Sleep Mode (<1μA)
- Fault Indication Output
- FCQFN(3mmx4mm) Package

APPLICATIONS

- Battery Power Tools
- Automotive High-Side Switches

TYPICAL APPLICATION



ORDERING INFORMATION

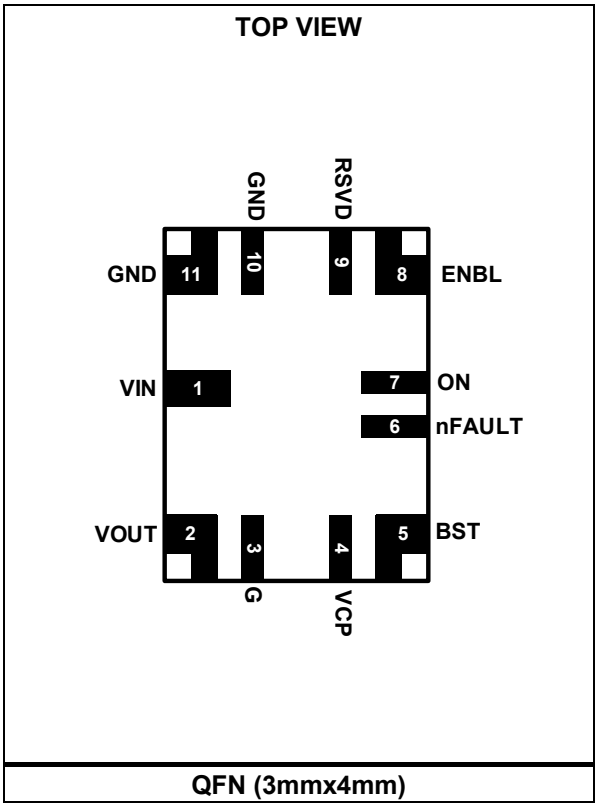
Part Number*	Package	Top Marking	MSL Rating
MP6590GLE	QFN (3mmx4mm) (wettable flank)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6590GLE-Z);

TOP MARKING

(TBD)

PACKAGE REFERENCE



QFN (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
7	ON	Input pin. High drives G to VIN + 12V; Low drives G to VOUT. Internal pull down resistor.
8	ENBL	Enable input. Low powers down device and drives G to VOUT. Internal pull down resistor.
6	nFAULT	Fault Indication. Open-drain output, logic low when in fault condition (OTP or UVLO).
2	VOUT	Connect to MOSFET source (switch output).
3	G	Connect to MOSFET gate.
5	BST	Gate drive power supply. Connect to a 100nF capacitor rated for at least 16V to VCP. See text.
4	VCP	Charge pump output. Connect to a 100nF capacitor rated for at least 16V to BST. See text.
1	VIN	Input Supply Voltage. Decouple to GND with minimum 100nF ceramic capacitor to GND. Additional bulk capacitance may be desirable.
9	RSVD	Reserved. Do not connect this pin.
10, 11	GND	System ground connection.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} .....-0.3V to 100V
VOUT, G Voltage .....-2V to 100V
VCP Voltage .....-0.7V to 100V
BST Voltage.....-0.7V to 100V
VOUT-G Voltage.....……..…-0.7V to 20V
All Other Pins to GND .....-0.3V to 6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
……...TBDW
Storage Temperature..... -55°C to +150°C
Junction Temperature..... +150°C
Lead Temperature (Solder)..... +260°C

ESD Rating

Human-body model (HBM) ..... 2000V(4)
Charged Device Model (CDM)……750V (5)

Recommended Operating Conditions

Supply Voltage V_{IN} (MP6590) .....7.5V to 80V
Supply Voltage V_{IN} (LV version) .....4.5V to 80V
Operating Junction Temp. (T_J). -40°C to +150°C

Thermal Resistance (3) θ_{JA} θ_{JC}

QFN (3mmx4mm).....TBD...TBD..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.
4) Per AECQ100-002
5) Per AECQ100-011

ELECTRICAL CHARACTERISTICS

V_{IN} = 14V, T_A = -40 to +150°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input Supply Voltage	V_{IN}	MP6590	7.5		80	V
		LV Version (metal option)	4.5		80	
Quiescent Current	I_Q	No load current, ENBL = 1		1.3	1.5	mA
	I_{SHDN}	Shutdown mode, ENBL = 0 25°C			2	µA
Gate Drive Output						
Output On Resistance	R_{PU}			400		Ω
	R_{PD}			10		Ω
Peak Output Current	I_{OUTP}			1		A
	I_{OUTP}			1		A
Control Logic						
Input Logic ‘Low’ Threshold	V_{IL}				0.8	V
Input Logic ‘High’ Threshold	V_{IH}		2			V
Logic Input Current	$I_{IN(H)}$	V_{IH}=5V	-20		20	µA
	$I_{IN(L)}$	V_{IL}=0.8V	-20		20	µA
Internal Pull Down Resistance	R_{PD}			500		kΩ
nFault Output (Open-Drain Output)						
Output Low Voltage	V_{OL}	I_O=5mA			0.5	V
Output High Leakage Current	I_{OH}	V_O=3.3V			1	µA
Protection Circuits						
UVLO Rising Threshold	V_{UV}	MP6590	6.6	7	7.4	V
		LV version (metal option)	3.7	4	4.3	
UVLO Hysteresis	ΔV_{UV}			500		mV
UVLO Blanking Time	t_{UVB}	From ON=1		20		µS
VCP Threshold Voltage	V_{VCPMIN}	MP6590	5.8	6.5	7.2	V
		LV version (metal option)	2.6	3	3.4	
Thermal Shutdown	T_{TSD}			180		°C
Thermal Shutdown Hysteresis	ΔT_{TSD}			25		°C
Charge Pump						
Gate Drive Output Voltage	V_{CP}	MP6590	VIN + 10.5	VIN + 12	VIN + 13.5	V
		LV version (metal option)	VIN + 4.5	VIN + 5	VIN + 6	

TIMING CHARACTERISTICS

V_{IN} = 14V, T_A = -40 to +150°C, unless otherwise noted.

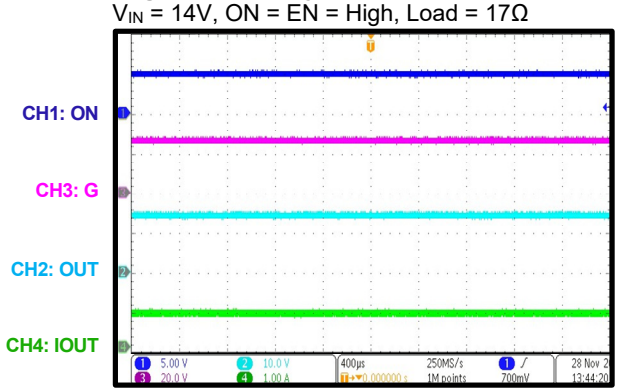
Parameter	Symbol	Condition	Min	Typ	Max	Units
Enable Time	t_{WAKE}	From ENBL = Low to High		50		µS
Disable Time	t_{SLEEP}	From ENBL = High to Low		200		nS
Power-up Time	t_{PUP}	From V_{VCP} > V_{VCPMIN}		200		nS
Propagation Delay	t_{PD}	IN to G=10V, C_L = 10nF		200		nS

TYPICAL PERFORMANCE CHARACTERISTICS

ON = 5V, EN = 5V, T_A = 25°C, unless otherwise noted.

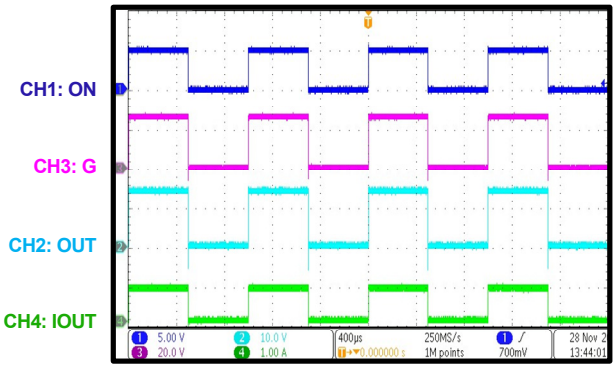
High-Side Fully On

V_{IN} = 14V, ON = EN = High, Load = 17Ω



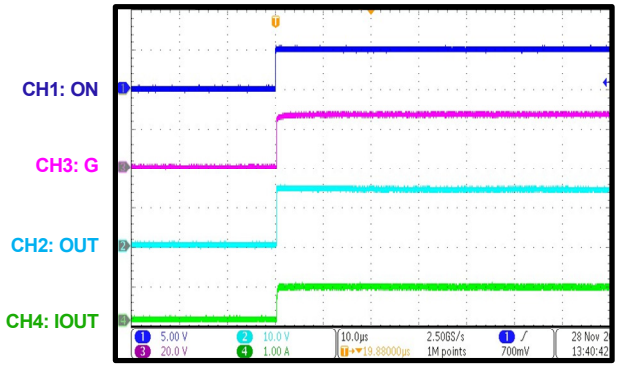
Switching Operation

V_{IN} = 14V, EN = High, ON = 1kHz/50%, Load = 17Ω



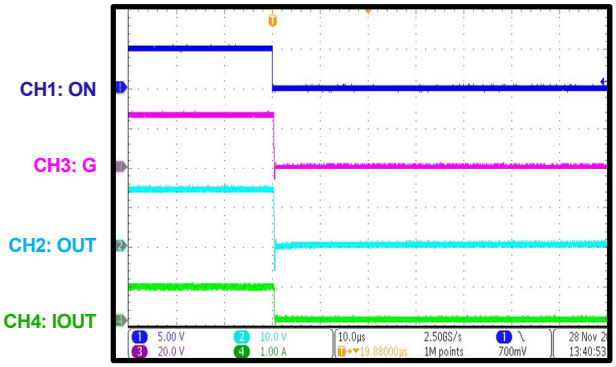
Turn on the MOSFET

V_{IN} = 14V, EN = High, ON from Low to High, Load = 17Ω



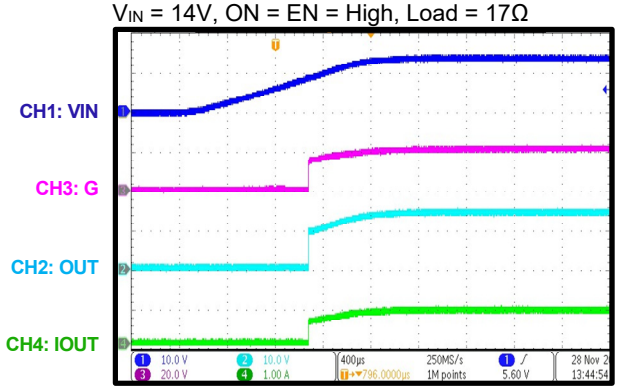
Turn off the MOSFET

V_{IN} = 14V, EN = High, ON from High to Low, Load = 17Ω



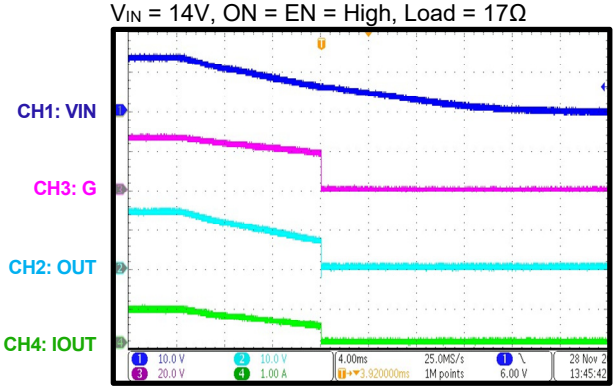
Start-Up through VIN

V_{IN} = 14V, ON = EN = High, Load = 17Ω



Shutdown through VIN

V_{IN} = 14V, ON = EN = High, Load = 17Ω

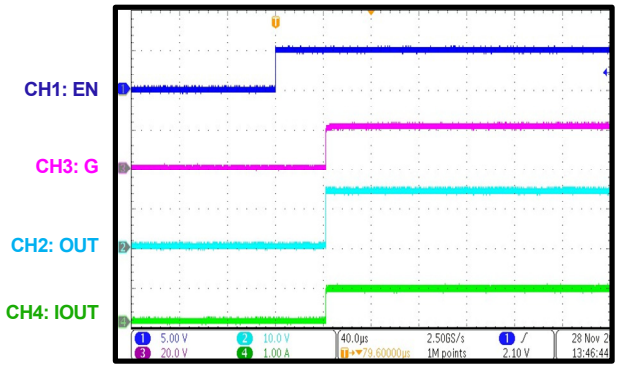


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

ON = 5V, EN = 5V, T_A = 25°C, unless otherwise noted.

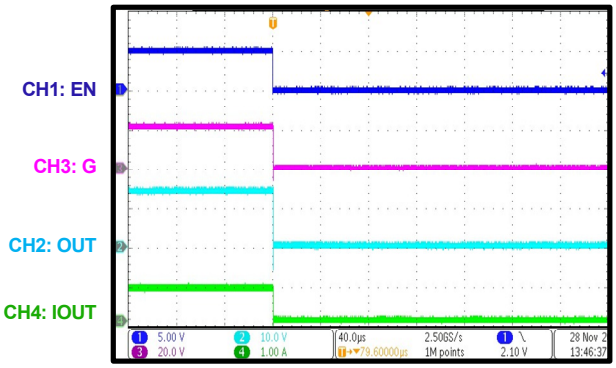
IC Enable

V_{IN} = 14V, ON = High, EN from Low to High,
Load = 17Ω



IC Disable

V_{IN} = 14V, ON = High, EN from High to Low,
Load = 17Ω



BLOCK DIAGRAM

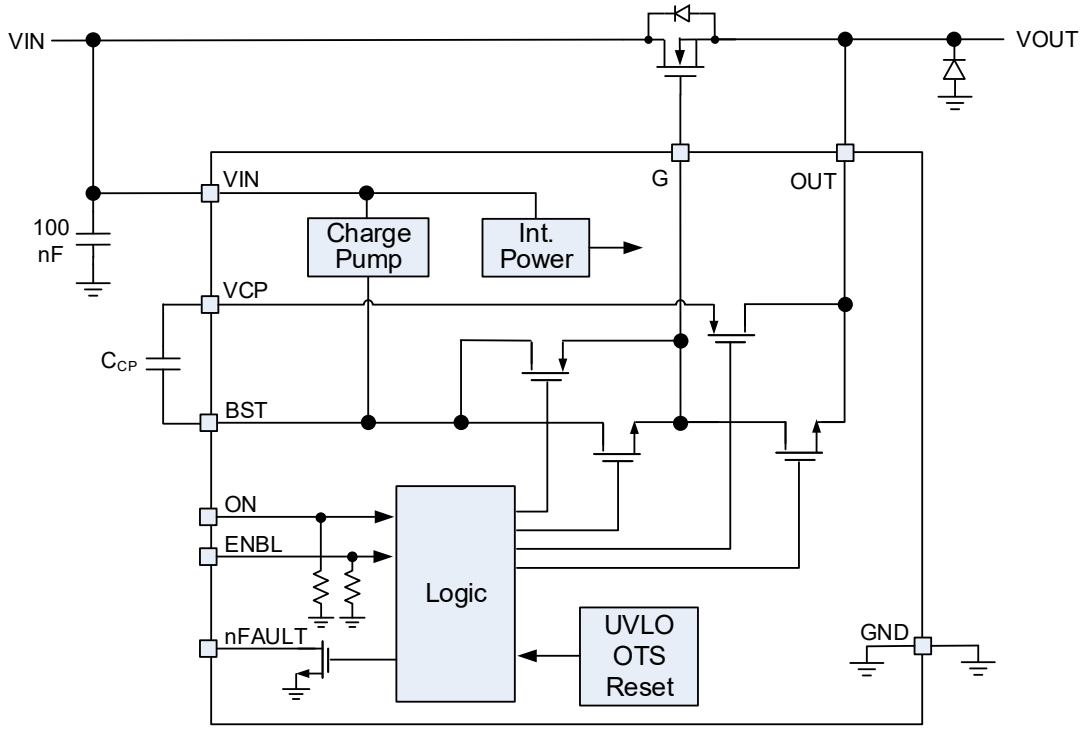


Figure 1: Functional Block Diagram

OPERATION

The MP6590, in combination with an external N-channel power MOSFET, is used to implement a high side switch. It generates the required gate drive voltage to fully enhance the external MOSFET, and provides control and protection functions.

Power-up

The MP6590 will start power-up when the VCP voltage exceeds V_{VCPMIN} and the ENBL pin is logic high. Turn-on of the external MOSFET is not allowed until VIN has exceeded the UVLO threshold V_{UVLO}, and the voltage at VCP has exceeded the V_{VCPMIN} threshold. There is a minimum delay of t_{PUP} before the MOSFET can be enabled to prevent rapid cycling in a fault condition.

Input Logic

The MP6590 has two input pins: ON and ENBL. Both pins have internal pulldowns.

The ENBL pin enables and disables the part. When ENBL is logic low, the internal charge pump is disabled and internal circuitry is put into a low power state. The G pin is pulled to VOUT to keep the external MOSFET disabled.

When ENBL is taken to logic high, the part is enabled and the charge pump runs.

The ON pin is used to turn the external MOSFET on. Logic high drives the G pin to VIN+12V (MP6590) or VIN+5V (LV version metal option) to turn the MOSFET on. Logic low drives G to VOUT to turn the MOSFET off.

Charge Pump / Bootstrap

An external capacitor is used as a bootstrap to initially turn on the external MOSFET. Once the MOSFET is on, a weak charge pump is used to overcome leakages to allow 100% duty cycle operation indefinitely.

Note that there must be some load at the OUT pin (MOSFET source) to return the current needed (approximately 10uA) to charge the bootstrap capacitor when the MOSFET is turned off. The load resistance must be less than (VIN-6.5V) / 10uA. This equates to 750kΩ at a VIN voltage of 14V.

The gate drive voltage is regulated at a nominal 12V for the standard MP6590. The LV version (metal option) lowers this voltage to 5V.

If the charge pump voltage drops to below the charge pump threshold voltage V_{VCPMIN}, the external MOSFET will be turned off.

Gate Driver

N- and P-channel FETs are used to drive the gate of the external MOSFET to either the charge pump voltage, or to the output, which is the source terminal of the external MOSFET.

A protective diode needs to be placed at VOUT pin to prevent the negative voltage which generated when the external MOSFET turn-off from damaging the MP6590.

VIN UVLO Protection

If at any time the voltage on the VIN pin falls below the under-voltage lockout threshold, the external MOSFET will be turned off, and the device will turn off most internal circuitry and enter a low power state. Operation will resume when VIN rises above the UVLO threshold.

UVLO protection is disabled for a short time t_{UVB} after the external MOSFET is turned on.

Overtemperature Protection

If the die temperature exceeds safe limits, the G pin will be driven to VOUT to turn the MOSFET off, and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

nFAULT Output

MP6590 provides an nFAULT pin which is driven active low if any of the protection circuits are activated. These fault conditions include a VCP undervoltage, VIN undervoltage, and overtemperature. nFAULT is an open-drain output and requires an external pullup resistor. When the fault condition is removed, the nFAULT pin is pulled inactive high by the pullup resistor.

APPLICATION INFORMATION

PCB Layout Guidelines

Proper PCB layout is critical to the performance of high-side gate driver. For the best results, refer to Figure 2 and follow the guidelines below:

1. Make the connection between the OUT pin and the MOSFET source as direct as possible to avoid excessive undershoot on the OUT due to inductive load or parasitic inductance.

2. Place the C_{BST} and supply bypass capacitors as close as possible to the IC.

3. Use wide copper areas for all the high current paths.

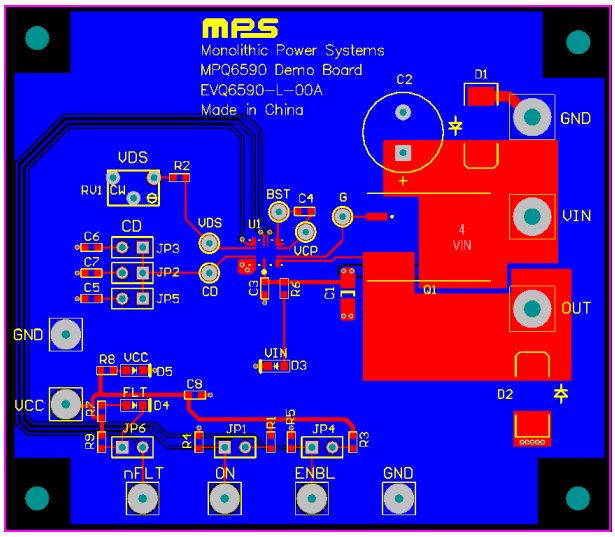
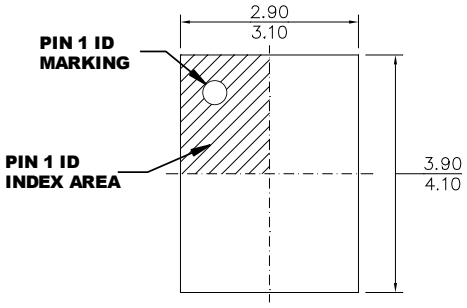


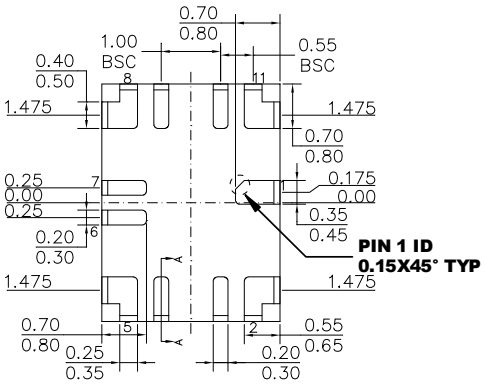
Figure 2

PACKAGE INFORMATION

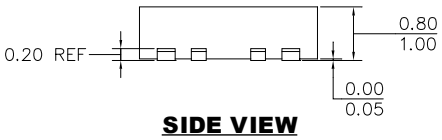
QFN 3mmx4mm
(wettable flank)



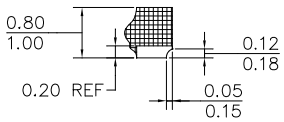
TOP VIEW



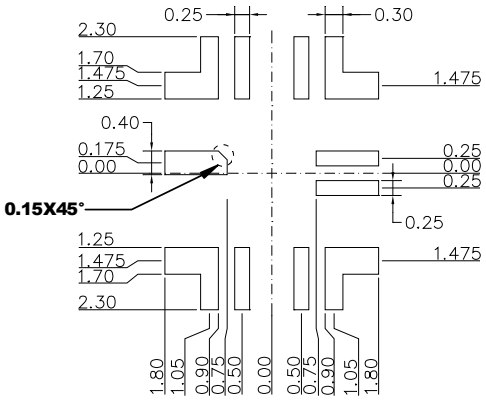
BOTTOM VIEW



SIDE VIEW



SECTION A-A

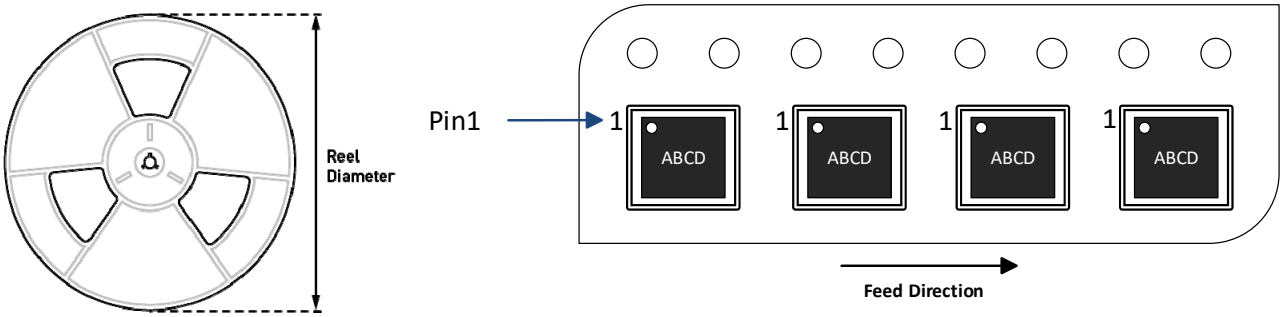


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6590GLE-Z	QFN (3mmx4mm) (wettable flank)	5000	N/A	N/A	13 in.	12 mm	8 mm